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SOFTWARE DEFINED RADIO RECEIVER PLATFORM BASED ON SIX-PORT TECHNOLOGY

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Cette thèse intitulée:

SOFTWARE DEFINED RADIO RECEIVER PLATFORM BASED ON SIX-PORT TECHNOLOGY

présentée par : Xin Yu Xu

En vue de l'obtention du diplôme de: Philosophiae Doctor

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To Linwen, Yunfan and my parents.

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RÉSUMÉ

Le radio logiciel (SDR) a été considérée comme une des techniques les plus vitales pour l'implémentation pratique des systèmes futurs de la communication sans fil. Dans le passé, la vitesse limitée d'opération pour le ADC et la capacité des traitements des puces re-configurables pour le traitement de signal digital faisait le développement lent du SDR pour l'application commerciale utile. Avec l'avancement récent de la technologie de traitement à semi-conducteur et le développement des mécanismes re-configurables tel que le DSP et le FPGA, le SDR est maintenant devenu les solutions pratiques pour beaucoup des systèmes commerciaux.

Actuellement, la plupart des systèmes au SDR numérisent le signal à la fréquence intermédiaire (IF), bien que le DSP et les technologies à semi-conducteur aient été développés rapidement dans le passé de dizaine années, c'est encore difficile au niveau de la vitesse d'opération des puces actuelles au DSP pour supporter complément les multi-canaux à la pleine vitesse et les multi-modes à IF. Sur l'intérim, les implémentations au SDR exigeront un mixage des techniques aux matériels intensifs tel que les ASICs. Les certains systèmes du radio à logiciel adoptent l'architecture aux multi-puces et aux algorithmes parallels, donc, augmentant la complexité de conception et le budget potentiel.

Au lieu des signaux à l'état de numérisation à la IF, les signaux aux micro-ondes / ondes millimétriques peuvent être numérisés à la base-bande avec la technologie six-port, donc réduisant l'exigence du traitement pour les puces au DSP. Cette nouvelle solution à la conception de SDR est basée sur la démodulation directe avec « la technologie six-port », convertissant-en bas directement le signal à la fréquence radio (RF) en la base-bande par le circuit six-port.

Cette dissertation décrit les travaux et les résultats en concevant un nouveau récepteur SDR basé sur la technologie six-port. Cet objectif du projet est de réaliser une application de SDR basé sur la technologie six-port pour fournir le récepteur digital aux multi-canaux et aux multi-modes directes sans fil dans les communications au masse-marché sans fil de la micro-onde / ondes millimétriques. Le circuit six-port est utilisé comme un mixage au lieu du circuit conventionnel à la RF, ce qui offre des plusieurs avantages importants tel que la simplicité, la petite volume, le budget en bas et les performances excellentes d'électricité. La combinaison du SDR et de la technologie six-port offre la flexibilité importante dans la configuration de système et la réduction considérable dans le budget du développement de système ainsi que la promesse très haute dans la re-utilisation de logiciel.

Comme les pièces principales de la tête de front du récepteur à la RF, deux différents types du circuit six-port ont été conçus avec la fréquence de centre à 24 GHz et la fréquence d'opération, sa bande de fréquence étant de 22GHz à 26GHz. Un s'est basé sur

la technologie hybride (MHMIC), et l'autre s'est basé sur la nouvelle technologie SIW. Les paramètres de dispersion de ces deux circuits six-port sont analysés et offerts.

Trois modulations QPSK, QAM16 et OFDM sont choisis pour tester la performance du récepteur. La conception et l'architecture fondamentales du récepteur six-port SDR étaient testées par l'exécution des simulations de circuit et de système utilisant une série de logiciels tel que le Agilent Advanced Design System (ADS), le High-Frequency Structure Simulator (HFSS), Mathworks Matlab et Simulink. La performance de simulation du récepteur du SDR est offerte ici, ce qui sont ensemble avec les différents modulations, la démodulation, l'analyse de la performance à noise et les algorithmes de calibration qui s'sont normalement associés à cette classe du récepteur. La plate-forme physique du récepteur six-port SDR est fabriquée s'étant basé sur les résultats simulés et les mesures de système sont exécutées pour confirmer la conception du récepteur.

Le récepteur proposé du SDR six-port a été prouvé adaptable pour les projets de la modulation, de la fréquence, de la phase et de l'amplitude. En comparant avec le récepteur traditionnel du SDR, le récepteur six-port a les avantages, desquels la bande de fréquence est plus large et le budget des circuits de la tête de front à la RF est plus bas ainsi que l'exigence de capacité de DSP plus bas aussi. Les résultats simulés et mesurés montrent que ce récepteur a les BER qui sont bas égal à 1E-6 pour E_b/N_0 de 11dB (pour « QPSK ») et 15dB (pour « QAM16 »). Le récepteur proposé du SDR six-port a été prouvé adaptable pour les différents projets de la modulation, ça montrant une

application possible d'un démodulateur direct pour les terminaux futurs de SDR dans les divers systèmes de communication, pour lesquels le budget est bas.

ABSTRACT

Software Defined Radio (SDR) has been considered as one of the most vital techniques for practical implementation of future wireless communication systems. In the past, limited operation speed of analog digital converter (ADC) and processing ability of re-configurable chips for digital signal processing slowed down the development of SDR for useful commercial application. With recent advance in semi-conductor processing technology and the development of re-configurable devices such as digital signal processors (DSP) and field programmable gate arrays (FPGA), SDR has now become practical solutions for many commercial communication systems.

Presently, most SDR system digitalized signal at intermediate frequency (IF), Although DSP and semiconductor technologies have been developed rapidly in the past ten years, it is still difficult for the operating speed level of current DSP chip to completely support a high-speed multi-channel and multi-mode SDR at IF level. In the interim, SDR implementations will require a mix of hardware-intensive techniques such as application-specific integrated circuits (ASICs). Certain software radio systems adopt multi-chips architecture and parallel algorithms, thereby increasing the design complexity and potential cost.

Instead of digitalizing signals at IF, microwave/millimeter wave signals can be digitalized at baseband with six-port technology, hence reducing the processing

requirement for DSP chips. This new solution to SDR design is based on direct demodulation with "six-port technology", down-converting radio frequency (RF) signal to base-band directly by a six-port circuit.

This dissertation describes the works and results in designing a new software defined radio digital receiver based on six-port technology. The objective of the project is to realize an application of SDR based on six-port technology to provide a multi-channel, multi-mode direct wireless digital receiver for microwave/millimeter wave wireless mass-market communications. Six-port circuit is used as a mixer instead of conventional RF circuit, which offers some important advantages, such as simplicity, small size, low-cost and excellent electrical performances. The combination of SDR and six-port technology provides great flexibility in system configuration, significant reduction in system development cost and very high potential for software reuse.

As principal components of receiver RF front end, two different types of six-port circuit have been designed with the center frequency of 24 GHz and operating frequency bandwidth from 22GHz to 26GHz. One is based on traditional miniaturized hybrid microwave integrated circuit (MHMIC) technology and the other based on a novel substrate integrated waveguide (SIW) technology. The scattering parameters of these two six-port circuits are analyzed and presented.

Three modulation schemes QPSK, QAM16 and OFDM are selected to test performance of the receiver. The basic concept and architecture of the SDR six-port receiver were tested by performing circuit and system simulations using a series of software such as the Agilent Advanced Design System (ADS), Ansoft High-Frequency Structure Simulator (HFSS), Mathworks Matlab and Simulink. The simulation performance of the SDR receiver is presented, along with different modulation schemes demodulation, noise performance analysis and calibration algorithms which are normally associated with this class of receiver. Based on the simulated results, a physical six-port SDR receiver platform is fabricated and system measurements are performed to validate the receiver design.

The proposed six-port SDR receiver has been proved adaptive for amplitude, phase and frequency modulation schemes. Compared with traditional SDR receiver, the six-port SDR receiver has wider bandwidth, lower cost for RF front-end circuits and lower DSP capability requirement. The simulated and measured results show that the receiver has bit error rates (BER) of as low as 1E-6 for E_b/N_0 of 11dB (for QPSK) and 15dB (for QAM16). The proposed six-port SDR receiver has been proved adaptive for different modulation schemes, showing a possible application of direct demodulator for future SDR terminals in various low cost communication systems.

CONDENSÉ EN FRANÇAIS

1. Introduction

Pour s'accommoder au développement rapide dans le domaine de la région de communication sans fil, y compris les réseaux de régions locales et le service personnel de communication, c'est nécessaire que l'on introduit une nouvelle architecture de communication qui offre la capacité plus grande et accommodate les spécifications des hardwares qui sont en état de changement toujours. Cette situation a amène le développement du radio logiciel (SDR), ce qui a beaucoup des fonctions définies par logiciel.

Le SDR est un radio, dans lequel les paramètres d'opération, y compris la portée de fréquence, le modulation ,ou la puissance de sortie qui est conduite ou émise au maximum peuvent être changés par la changement de logiciel sans aucun changement de hardware. L'essence d'un SDR, c'est la capacité, sans introduire des nouveaux hardwares , pour changer des caractéristiques d'opération en changeant les programmes de logiciel qui sont en train d'exécuter dans les ressources de traitement. Ça permet au seul appareil sans fil d'être reprogrammé pour utiliser les différentes modulations, différents codages et différents protocoles d'accès.

2. Récepteur du Radio logiciel

Un point clé de SDR, c'est de posséder le chenil de traitement digital avec la capacité presque infinie. Bien que le DSP et les technologies à semi-conducteur aient été développés rapidement dans le passé de dizaine années, c'est encore difficile que le niveau de la vitesse d'opération de la puce courante du DSP supporte complètement un multi-canal avec une haute vitesse et une multi-mode du SDR au niveau de la fréquence intermédiaire (IF). Dans l'intérim, l'implémentation de SDR exigera un mixage de techniques à hardware-intensive tel que les ASIC. Certain systèmes du radio à logiciel adoptent l'architecture aux multi-puces et aux algorithmes parallels, donc augmentant la complexité de conception et le budget potentiel aussi.

Au lieu des signaux à l'état de numérisation à la IF, les signaux à micro-onde/ondes millimétriques peuvent être numérisées à base-bande avec la technologie six-port, donc réduisant l'exigence du traitement pour puces de DSP. Cette nouvelle solution de la conception pour le SDR s'est basée sur la démodulation directe avec « la technologie six-port », convertissant--en bas directement le signal en fréquence radio(RF) à base-bande par le circuit six-port.

Une plate-forme du récepteur du SDR qui s'est basée sur la technologie six-port est présentée dans cette dissertation. L'objectif des travaux est de réaliser une application de SDR et de fournir le récepteur digital direct sans fil à multi-canal et à multi-mode. Le

circuit six-port est utilisé comme un mixage au lieu du circuit conventionnel à la RF, ce qui offre des plusieurs avantages importants tel que la simplicité, la petite volume, le budget bas et des performances excellentes d'électricité. La combinaison du SDR et la technologie six-port fournit la flexibilité importante dans la configuration de système et la réduction considérable dans le budget du développement de système ainsi que la promesse très haute dans la re-utilisation de logiciel.

3. Principe d'opération du récepteur six-port

La technologie six-port a été en cours du développement à travers du passé de trente années pour les applications de mesure de micro-onde et de ondes millimétriques. En 1994, Ji Li, R. G. Bosisio et Ke Wu proposaient une application de cette technologie pour le récepteur direct. Par principe, le système de circuits d'un six-port consiste en les diviseurs à signal et les combinaisons (ou les coupleurs) à signal qui sont reliées de telle façon que quatre sortes de différents calculs du signal à référence et le signal à être mesuré sont produits. Les pièces sont raccordées par des lignes de transmission avec des différentes longueurs. Les deux signaux de données en entrée généré les différentes valeurs de phase aux ports de sortie en entraînant une interférence constructive ou destructive. Les niveaux des quatre signaux combinés sont détectés en utilisant les détecteurs de puissance. Si on raccorde le port 1 au signal LO, port 2 au signal RF reçu en appliquant les algorithmes adéquats, l'ampleur et la phase du signal RF inconnu peuvent être déterminés pour le projet déjà donné de modulation des quatre valeurs de

puissance et les coefficients de calibrage qui sont obtenus par ces signaux qui sont arrivés.

Comme on sait, les convertisseur-en bas à large bande ne sont pas disponible facilement aux fréquences à millimètre onde. Dans le récepteur six-port SDR, le circuit six-port plus les détecteurs travaillent comme un convertisseur-en bas, ce qui offre une voie rentable d'accès pour convertir en bas directement le signal à la RF en le signal à base-bande. De plus, les signaux à base-bande, dans lesquels la fréquence est bas relativement, réduisent l'exigence de capacité au DSP et d'échantillonner ADC. D'un autre côté, le récepteur six-port a besoin d'un ensemble de 4 BPF et ADC, ce qui augmente potentiellement le budget de système, cependant, avec le développement récent de la technologie ASIC le budget de cette pièces sera considérablement réduit.

Le récepteur six-port SDR proposé a été prouvé adaptable pour les modulations à la fréquence, de la phase et de l'amplitude. En comparant avec le le récepteur traditionnel au SDR, le récepteur six-port a les avantages, desquels la bande de fréquence est plus large et le budget pour l'utilisation des circuits à la RF de la tête de front est plus bas ainsi que l'exigence de capacité au DSP plus bas aussi. Pour certains modulations(par exemple QPSK) il y a les algorithmes de démodulation rapide pour le récepteur six-port, ce qui rend la code de démodulation au DSP très simple.

La plate-forme du récepteur SDR, c'est la combinaison de l'étage à la RF et l'étage à base-bande. Dans l'étage à la RF le circuit six-port plus les détecteurs travaillent comme un convertisseur en bas qui convertit en bas directement le signal reçu de la fréquence à RF en la base-bande. L'étage à la base-bande comprend les amplificateurs à la base-bande, les filtres à passe basse(LPF) à la base-bande, ADCs et DSPs. Les DSPs sont la partie la plus importante du récepteur SDR. C'est responsable pour le traitement du signal à base-bande tel que la démodulation et le décodage.

4. Circuit six-port

Comme les pièces principales de la tête de front du récepteur à la RF, deux différents types du circuit six-port ont été conçus avec la fréquence de centre de 24 GHz et la fréquence d'opération à bande de fréquence de 22GHz à 26GHz . Un s'est basé sur la technologie du circuit traditionnel dans laquelle la technologie hybride (MHMIC) et l'autre basé sur la nouvelle technologie de SIW.

Circuit six-port de la microstrip

En utilisant le Advanced Design System (ADS)de logiciel de Agilent Technologies, un circuit de microstrip à six-port a été conçu et fabriqué à la fréquence de centre de 24 GHz avec des bande de fréquence de 22 GHz à 26 GHz. Le circuit six-port consiste en un Wilkinson coupleur (travailler comme un diviseur de puissance) et trois coupleurs de

hybride pour quadrature. Se référant à la conception de circuit six-port pour S. O. Tatu's 27 GHz, Le circuit (proposé) à six-port est fabriqué avec la technologie MHMIC sur un substrat céramique, son épaisseur étant 0.254 mm, avec la permittivité relative εr = 9.9. La puce de MHMIC mesure 9.5x8.4 mm. La longueur correspondante à fréquence de centre est 4.73 mm. Les paramètres de dispersion de circuit(proposé) de microstrip à six-port sont simulés en utilisant ADC et mesurés avec une test fixture de Anrithsu et un analyseur de réseaux de type HP-8510.

Ça peut être trouvé de ces résultats qui sont simulés et mesurés et qui ,par-dessus la bande de fréquence d'opération, le circuits six-port proposés va bonnes adaptations (S11, S22, S33, S44, S55, S66 sont moins que -20dB) et isolations (S12, S34, S35, S36, S45, S46, S56 sont moins que -20dB). Pendant que les paramètres de transfert (S31, S41, S51, S61, S32, S42, S52, S62) sont très proche aux valeurs théoriques.

Circuit six-port SIW

Le SIW est un type de l'onde guide rectangulaire qui est de diélectrique-rempli et qui est synthétisée dans un substrat plate avec les tableaux métalliques de passages pour réaliser les murs de tranchant bilatéral, et ses transitions avec les structure plates sont conçues et intégrées sur le même substrat. Dans ce cas, les deux sortes des structures plates et celles non-plates peuvent être intégrées dans la même plate-forme plate, ce qui entraîne à la conception et au développement des circuits intégrés (ICs) et des systèmes coût réduit

dans lesquels l'ondes millimétriques. Avec les structures de le SIW, un système peut être intégré même dans un papuet, donc réduisant la volume, le poids , le prix et améliorant considérablement la répétition de fabrication et la fiabilité.

S'étant basé sur cette propriété de le SIW, les techniques actuelles de conception à onde guide rectangulaire peuvent être utilisées de la façon directe pour analyser et concevoir des diverses pièces en savant la largeur effective de le SIW. Un nouveau circuit six-port SIW est conçu s'étant basé sur la technique actuelle de l'onde guide rectangulaire. En utilisant le HFSS, un circuit six-port est conçu à la fréquence de centre de 24 GHz avec des bande de fréquence 22 - 26 GHz. Le circuit est fabriqué sur un substrat, pour lequel l'épaisseur 0.508 mm, Rogers RT/duroid 5880 une plaque laminé, avec la permittivité relative $\varepsilon r = 2.2$. Ça consiste en deux diviseurs de puissance de le SIW et deux coupleurs de hybride de le SIW ainsi que le leviers de vitesse de plusieurs phases. Comme des blocs fondamentals de construction du circuit six-port le diviseur de puissance de le SIW, le coupleur de hybride de le SIW de 3 dB et une transition avec des structures plates sont conçus.

Paramètres de dispersion S du circuit six-port proposé sont simulés en utilisant HFSS et mesurés par un analyseur de réseau HP-8150. Les résultats simulés et mesurés sont d'accord très bien, montrant que le circuit six-port proposé va bonnes adaptations (S11, S22 sont moins que -20 dB à la fréquence de centre de 24 GHz), et isolations des deux ports entré est excellent (S12 est moins que -20 dB at 24 GHz). En même temps les

paramètres de transfert (S31, S41, S51, S61, S32, S42, S52, S62) sont très poche aux valeurs théoriques.

5. Algorithmes de récepteur

Le tableau de circulation du récepteur six-port SDR peut être décrit comme suivant: après informations sont appris de l'antenne, certaines échantillons sont choisies pour la calibration. De cette calibration, les coefficients de calibration à six-port peuvent être générés. Ces coefficients sont alors appliqués dans le calcul pour calculer les données I-Q. En suivant un algorithme de décision, les signaux sont alors démodulés . Ce processus est un algorithme universel de démodulation pour les récepteurs six-port. Cependant, dans certains cas, par exemple pour certains projets de démodulation, les coefficients de calibration n'est pas nécessaire pour le calcul de six-port. De cette façon, la procédure de calibration peut être omis et l'algorithme de démodulation puisse être simplifié.

Beaucoup de algorithmes ont été proposés pour la calibration de réflectomètre six-port dans le passé de trente années. Normalement cettes méthodes de calibration à six-port utilisent les terminaux physique extérieur de standard qui sont raccordés à ses ports de données en entrée. Cependant, pour un récepteur sans fil, c'est peut-être entièrement irréaliste. Donc dans le récepteur proposé, on adopte une méthode de calibration en temps réel qui est débarrassée d'aucun raccordement extérieur. Les coefficients de

calibration peuvent être déterminés des quatre différents états des signaux modulés, alors les calculs du récepteur de sortie I, Q données peuvent être faits utilisant les proportions des indications de sortie pour le détecteur de puissance.

6. Performance de récepteur

À l'intérieur de la bande de fréquence d'opération du récepteur, les trois modulations QPSK, QAM16 et OFDM sont choisis pour tester la performance du récepteur sur la phase, l'amplitude et des modulations de fréquence. La conception et l'architecture fondamentale du récepteur six-port SDR étaient testées en exécutant les simulations de système et de circuit en utilisant une série des logiciels tel que le Advanced Design System (ADS) de logiciel de Agilent technologies, le High-Frequency Structure Simulator (HFSS) de Ansoft, Mathworks Matlab et Simulink. La performance de démodulation du récepteur SDR est présentée, avec des différents modulations, la démodulation, l'analysais de la performance de bruit et les algorithmes de calibration qui se sont normalement associés à cette classe du récepteur. S'étant basé sur les résultats simulés, une plate-forme physique du récepteur six-port SDR est fabriquée et les mesures de système sont exécutés pour confirmer la conception du récepteur.

Les résultants de la démodulation simulés montrent que le récepteur a une précision de ± 5 degrés sur la phase et ± 0.2 dB sur l'amplitude pour la modulation QPSK et ± 5 degrés sur phase et ± 0.4 dB sur l'amplitude pour modulation QAM 16.

Les résultants simulés et mesurés montrent que le récepteur a taux d'erreur de bit (BER) qui est aussi bas que 1E-6 pour E_b/N_0 de 11dB (for QPSK) et 15dB (for QAM16). pour le signal OFDM, les résultats simulés montrent que le signal peut être démodulaté même le rapports signal/bruit (SNR) est aussi bas que 0 dB.

7. Conclusion

Une plate-forme universel du récepteur SDR s'étant basé sur la technologie six-port a été proposée et présentée ici. Ce récepteur peut supporte la communication à multi-bande et à multi-modulation et a l'intention d'accomplir la performance comparable que possède le récepteur actuel du récepteur super-hétérodyne. Ce projet de la plateforme est vivement motivé par le fait pour lequel la vitesse et la performance de l'état d'art des instruments re-configurable, tel que le DSP et le FPGA, sont plein de promesses et le prix sera considérablement réduit, pendant que le budget des pièces de la micro-onde sont stable relativement. La configuration du récepteur déplace la complexité pour la partie de traitement de signal digital et réduit des problèmes qui sont associés avec des composante à RF; donc ça va être aisé selon le budget et la fonction à long terme.

Ce travail de recherche qui est décrit par cette dissertation a construit une espace entre la technologie six-port et le champ du SDR en l'état d'émergence. Ça est prouvé à travers d'un certain nombre des simulations et mesures qui sont faites par ordinateur, dans

lesquelles la combinaison du SDR et la technologie six-port offre une grande flexibilité sur la configuration de système, une réduction considérable sur le budget au développement de système, et une promesse haute sur la re-utilisation de logiciel aussi. Ce récepteur six-port SDR proposé a été prouvé adaptable pour les différents modulations, ça montrant une application possible de démodulation directe pour les terminaux futurs du SDR dans le système de communication avec des divers budgets bas.

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LIST OF ACRONYMS AND ABBREVIATIONS

1G	First Generation
2G	Second Generation
3G	Third Generation
ADC	Analog Digital Converter
ADS	Advanced Design System
ASIC	Application-Specific Integrated Circuit
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BI-RME	Boundary Integral – Resonant Mode Expansion
BPF	Band Pass Filter
CPU	Central Processor Unit
CPW	Coplanar Waveguide
DAB	Digital Audio Broadcasting
DAC	Digital-to-analog converter
DSP	Digital Signal Processor
DUT	Device Under Test
FCC	Federal Communications Commission
FEM	Finite Element Method
FFT	Fast Fourier Transform

FPGA	Field Programmable Gate Arrays
GP	General Purpose
GPS	Global Positioning System
HFSS	High-Frequency Structure Simulator
IC	Integrated Circuit
IF	Intermediate Frequency
ISI	Inter Symbol Interference
ITS	Information Transfer System
JTRS	Joint Tactical Radio System
LAN	Local Area Network
LMCS	Local Multipoint Communication System
LO	Local Oscillator
MFLOPS	Millions of Floating-Point Operations Per Second
MHMIC	Miniaturized Hybrid Microwave Integrated Circuit
MIPS	Millions of Instructions Per Second
MMIC	Monolithic Microwave Integrated Circuit
MSAT	Mobile satellite
OFDM	Orthogonal Frequency Division Multiplexing
OTA	Over the Air
PCB	Printed Circuit Board
PCS	Personal Communications System / Service
PDA	Personal Digital Assistant

PLD	Programmable Logic Device
PPDR	Public Protection and Disaster Relief
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RMS	Root Mean Square
SDR	Software Defined Radio
SIW	Substrate Integrated Waveguide
SOP	System On Package
SPR	Six-Port Reflectometer
SNR	Signal-to-Noise Ratio
WLAN	Wireless Local-Area Network

CHAPTER I

INTRODUCTION

To adapt the rapid development in wireless communication area including local area networks (LAN) and personal communication service (PCS), it is necessary to introduce a new communication architecture that offers greater capacity and can accommodate the ever-changing hardware specifications. This has led to the development of the Software Defined Radio (SDR), a radio which has much of its functionality defined in software.

An SDR is a radio which the operating parameters, including the frequency range, modulation scheme or maximum radiated or conducted output power can be altered by making a change in software without making any hardware change [1]. The essence of an SDR is the ability, without introducing new hardware, to change operating characteristics by changing the software programs executing in processing resources. In an SDR, operating parameters are determined by software. This enables a single wireless device to be reprogrammed to use different modulation, coding, and access protocols.

Figure 1.1 shows a block diagram of an ideal SDR. Broadband RF signals are converted to base-band and fed to high speed ADC and programmable digital filter or channel decoder to select the desired channel signals. The transmission rates and modulation schemes are readily programmed. The hardware for this procedure requires down-

conversion to base-band of the entire bandwidth for various mobile standards and different frequency bands. This base-band signal is digitalized and all the subsequent processing is implemented in software [1], [3]-[5].

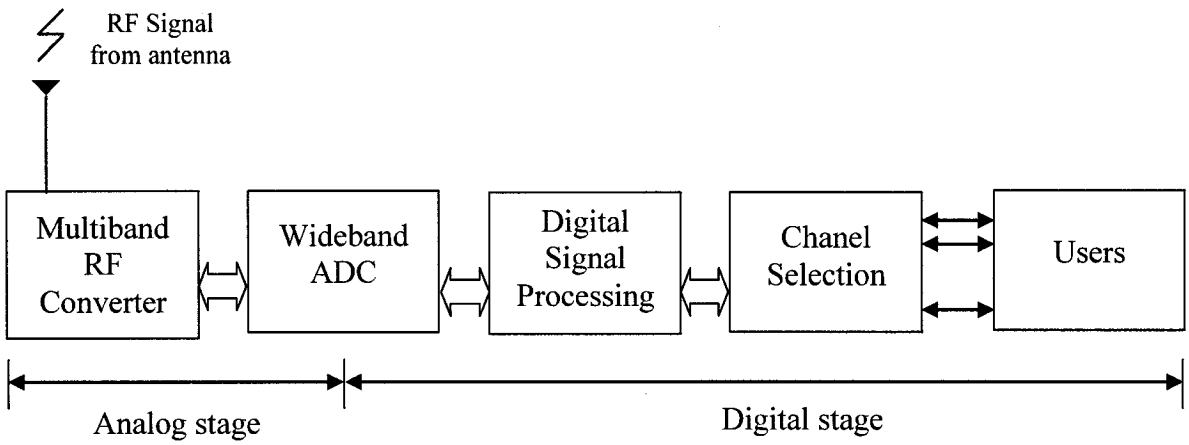


Figure 1.1 Block diagram of a Software Defined Radio receiver

SDR allows more efficient use of spectrum by facilitating spectrum sharing and by allowing equipment to be reprogrammed for various modulation schemes. The ability of SDR to be programmed also enhances interoperability between different radio services.

An ideal SDR receiver must be wideband with high-speed ADCs and effective operating algorithms. Data signals from antenna are converted from analog to digital, and remaining tasks are processed in the DSP. Limited by the ability of current ADC and re-programming device, present SDR receiver systems convert signals from analog to digital after frequency down-conversion from RF to base-band or IF.

SDR can be considered to be an information transfer system (ITS) combining technology from historically separate fields of computers and radios. Emerging from military applications, SDR has received much attention by researchers who investigate wireless communications; moreover, several websites [6]-[8] are providing details of SDR systems. Taking advantage of state-of-the-art digital signal processing technology, the performance of SDR systems depends more on DSPs and low cost RF hardware. Therefore, SDR systems can be achieved by less stringent requirements for expensive RF circuit fabrication and more flexibility for diverse communication systems.

SDR has been identified as a potential method to enhance flexible wireless communication systems. The operation speed of an Analog Digital Converter (ADC) and processing ability of digital signal processors (DSPs) and chips are the key factors in the development of SDR for useful commercial applications. Recent progress in semi-conductor processing technology and the development of re-configurable devices such as digital signal processors (DSPs) and field programmable gate arrays (FPGAs) reduce the development life cycle of commercial products. An SDR receiver platform based on six-port technology is presented in this dissertation. The objective of the works is to realize an application of SDR and provide a multi-channel, multi-mode wireless direct digital receiver. As we know from new studies of the use of six-port technology [9] in various design aspects for a new SDR receiver, SDR in conjunction with six-port

technology has promising applications in wireless LANs, audio and television broadcasting, and interoperability between different radio services.

The combination of SDR and six-port technology provides great flexibility in system configuration and significant reduction in hardware cost, particularly at millimeter wave frequencies potential for software reuse. The six-port receiver approach offers wide band accommodation to ever-changing communication specifications required in an SDR and has already been demonstrated with wide bandwidth from 2 MHz to 2200 MHz [10], 0.5GHz to 9GHz and 22GHz to 31GHz [11].

In the past years, different types of six-port circuits have been designed at the Poly-Grames research center, with center frequencies at 2.4 GHz, 5.8 GHz, 24 GHz and 28 GHz [12]-[14], operating over large frequency bands. Some six-port circuits are based on micro-strip structures, fabricated with MHMIC or monolithic microwave integrated circuit (MMIC) technology at both microwave and millimeter wave frequencies. Other circuits use a novel SIW structure [15] which allows integration of planar integrated circuit structure with waveguide structure. The performances of these six-port circuits in digital receivers are reported and published in relation to signal modulation schemes, noise performance analysis, calibration methods, and coding technologies. Simulated and measured BER results obtained with demodulation algorithms are given for QPSK, QAM16 and OFDM signals under a variety of operating conditions. It shows that this type of receiver can provide bit error rates as low as 1E-6 for E_b/N_0 of 11dB (for QPSK),

15 dB (for QAM16). Initial results show promising applications of six-port technology for direct conversion demodulation reception, which are needed in future low cost SDR communication systems [16]. Measured and simulated demodulation results of the proposed six-port SDR receiver are given in Chapter VII.

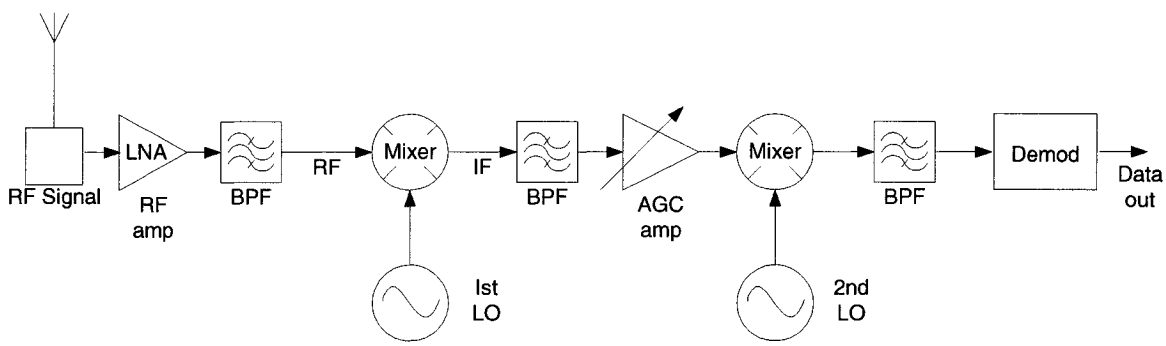


Figure 1.2 Block diagram of typical super-heterodyne digital receiver

In general, digital receivers that are used in RF communication systems can be divided into two categories: super-heterodyne receivers and direct conversion receivers. Figure 1.2 as mentioned, illustrates a simplified block diagram of a typical super-heterodyne digital receiver. The received RF signal is first amplified and then down-converted to a lower frequency (IF). Desired signal is filtered to eliminate noise and interference and a succeeding high-gain AGC amplifier stabilizes the output signal level since the input RF signal level may vary due to a fading transmission channel. The super-heterodyne receiver has advantages such as high sensitivity, high frequency selectivity. It has become the de facto standard configuration in most communication systems. However,

this kind of receiver uses many components including several band-pass filters (BPF) and IF amplifiers, and it is less suited for high level circuit integration and fabrication means that are needed for SDR mass production markets.

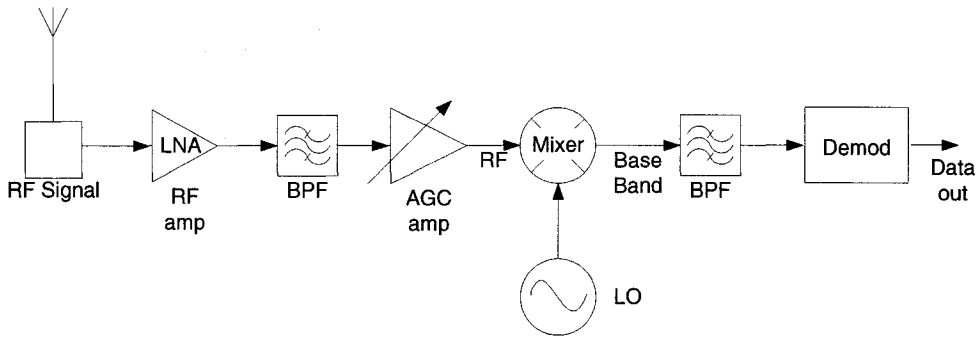


Figure 1.3 Block diagram of typical direct digital receiver

On the other hand, Figure 1.3 shows the block diagram of a typical direct digital receiver. The received RF signal is converted by a mixer directly from RF to base-band. The direct conversion receiver offers several advantages: it is simpler and less costly than super-heterodyne receiver, since no IF amplifier, IF band-pass filter, neither IF local oscillator are required for final down conversion. Therefore, the overall configuration of the direct receiver is expected to be much simpler than the super-heterodyne receiver, leading to a potential cost-effective solution. Another important advantage of direct conversion is that there is no image frequency. Since the mixer difference frequency is effectively zero, the sum frequency, which equals to two times the LO frequency, is easily filtered. However, one important disadvantage of direct receivers is that the LO

must be very stable, and it is hence costly, especially for millimeter wave frequencies. In addition, wideband down-converters are not readily available at millimeter wave frequencies. An alternative method is the use of six-port based, direct digital receiver architecture (Figure 1.4). Recent results [17], [18] with carrier recovery from QPSK signals offer an interesting approach used in six-port type receivers to reduce LO costs without imposing serious limits on wideband operation.

The six-port based SDR receiver shown in Figure 1.4 uses direct conversion scheme, the base-band signal is digitalized at four output terminals of the six-port circuit. The proposed six-port based digital SDR receiver targets multi-modulation and multi-band wireless communication systems at low cost for mass-market millimeter wave applications. It consists of a new broadband RF converter followed by re-configurable devices. The RF converter employs the direct conversion approach using a six-port circuit at 24 GHz.

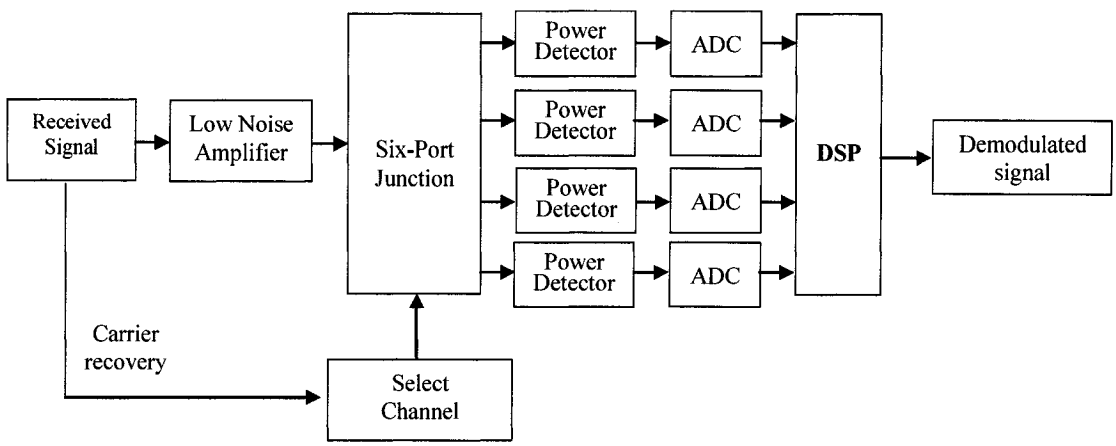


Figure 1.4 Block diagram of typical direct six-port SDR receiver

The concept of the six-port based receiver is derived from six-port technology, which is developed as an amplitude and phase measurement methodology for high frequency signals [19]. In 1994, an idea of six-ports for direct receivers was proposed for the first time in Poly-Grames research center of École Polytechnique de Montréal [2]. Several six-port receivers have been developed since then for microwave and millimeter wave communications. Carrier recovery method for six-port receiver has advanced and LO frequency can be retrieved from the RF input by carrier recovery means [11], [20]. Six-port receivers have been proposed for being robust, and having low manufacturing cost and low power consumption. More investigations are however needed and present studies indicate that a six-port receiver has a strong potential to solve a number of current communication and marketing problems, including multi-user modulation, seamless radio reception, low cost and wide band operation.

The dissertation is organized in the following way:

Following this brief overall introduction, chapter II presents the concept of Software Defined Radio. The systematic architecture of SDR is presented. The DSP section in SDR system, advantage and limitation of six-port SDR systems and broader implications of SDR are discussed. It also compares the software receiver with the conventional hardware receiver.

Chapter III introduces the operating principle of six-port receiver. The concept of six-port technology and the characteristic of six-port circuit are described. The advantage and disadvantage of the six-port SDR receiver comparing with typical SDR receiver have been discussed.

Chapter IV describes the optimum design of microstrip six-port circuit. Layout of the six-port circuit has been presented and the simulated and measured scattering parameters of the microstrip six-port are also given.

A new Substrate Integrated Waveguide (SIW) six-port circuit is proposed in Chapter V. The millimeter wave six-port junction based on the SIW technology is proposed and presented for the first time. The circuit layout, S-parameters and comparison of microstrip six-port and SIW six-port are given.

Chapter VI is about receiver algorithms. Six-port calibration methods (both offline and online) are presented. DSP algorithms that allow coherent demodulation for phase, amplitude and frequency modulation scheme are described. Simplified demodulation algorithms for certain modulation schemes are discussed at the end of the chapter. This chapter highlights the advantage of DSP in SDR communication systems.

Chapter VII describes simulated and measured demodulation results for the proposed SDR receiver. The bit error rate (BER) performance of SDR receiver for different

modulation schemes (QPSK, QAM16 and OFDM) schemes with simulated and measured results are described.

Chapter VIII is the conclusion as well as the future tendency of six-port SDR receivers

CHAPTER II

SOFTWARE DEFINED RADIO

2.1 Current Status of Software Defined Radio

Important strides have been made in the development of SDRs over the past few years. With significant progress in reconfigurable logic technology, SDR enabled cellular base stations began to dot the landscape. In addition, the public safety community continues to view SDR as a potential solution for its interoperability challenges in public protection and disaster relief (PPDR).

Today, we're seeing SDR products emerge in every sector of the industry. The focus has shifted to implementation and applications and bringing products to market. The major military equipment providers have products that they tout as SDRs, and they are being encouraged by the joint tactical radio system joint program office (JTRS JPO) to conform to common standards and to adopt the software communication architecture as the operating system for their radios. The evolution toward practical software radios is accelerating through a combination of techniques. These include smart antennas, multi-band antennas, and wideband RF devices.

The capabilities of digital logic have progressed to the point that it is now possible to cope with the signal and data processing requirements of SDRs with a variety of implementations. Nowadays wideband ADCs and digital-to-analog converters (DACs) can access GHz of spectrum instantaneously, IF, base-band, and bit stream processing is implemented in increasingly general-purpose programmable processors with application-specific integrated circuits (ASICs), field programmable gate arrays (FPGAs), digital signal processors (DSPs), and general-purpose processor technologies are being introduced in SDR designs. SDR is becoming practical as costs per millions of instructions per second (MIPS) of DSPs, and general-purpose central processor units (CPUs) have dropped below $10 per MIPS. The economics of software radios become increasingly compelling as demands for flexibility increase while numerical processing costs continue to drop by a factor of two every few years but RF parts and sub-assembly costs tend to remain high particularly at millimeter wave frequencies. At the same time, absolute processing capacities continue to climb from the hundreds of millions of floating-point operations per second (MFLOPS) to billions of FLOPS (GFLOPS) per chip. At present time, software radio technology can be cost-effectively implemented for commercial first-generation (1G) analog and second-generation (2G) digital mobile cellular radio air interfaces. Over time, wideband third generation (3G) air interfaces will also yield to software techniques on wideband RF platforms possibly at millimeter wave frequencies. The resulting SDR extends the evolution of programmable hardware, increasing flexibility via increased programmability. The ideal software radio represents the point of maximum flexible programmability in this evolution.

In addition, ADCs and DACs are available as low-cost chips and single-board open-architecture configurations offer bandwidths of tens of MHz with the dynamic range required for software radio applications. Multimedia requirements for desktop and wireless personal digital assistants (PDAs) continue to exert downward pressure on parts count and on power consumption of such chip sets. This trend will push the ideal software radio technology from the base station to the mobile terminal. Although the tradeoffs among analog devices, low-power ASICs, DSP cores, and embedded microprocessors in handsets remain fluid, cutting-edge base stations are beginning to employ software radio architectures. New designs for high-end mobile radio nodes such as military vehicular radios are now largely based on some type of software radio approach. Finally, the multi-band, multi-mode, and multi-user flexibility of software radios appears central to the goal of seamless integration of personal communications systems (PCS), land mobile and satellite mobile services.

In parallel with the evolutionary progress of software radio technology, in September 2001, the U.S. federal communications commission (FCC) formally recognized the role of regulation in facilitating the deployment of SDRs when it issued the First Report and Order (FCC 01-264) to allow manufacturers to make software changes in radios without requiring new equipment authorization applications. This, in part, focused on the immediate challenge of fixing "bugs" in radio software by permitting downloading of software over the air, while taking measures to prevent unauthorized download of

software. In that same proceeding, the FCC allowed for electronic labelling so that software changes would not be necessary to return the equipment to the manufacturer for re-labelling to indicate compliance with standards. These new rules not only facilitate over the air (OTA) software download, but the commission feels that using software defined radios will "facilitate more efficient use of the spectrum."

2.2 Software radio and hardware radio

Comparing with the traditional hardware radio, SDR has various advantages; the main advantage of software radio is its flexibility. Nowadays, with rapid developments in the wireless communication area, there are many communication schemes and standards while at the same time, new technologies, communication schemes and standards are under development. The new technologies ask for a new system structure. The new system structure should have greater capacity for new schemes and standards. It should accommodate the ever-changing hardware specifications, and can work as a bridge for different radio systems as well. SDR is considered the most possible answer of the new system. It is supportable for various radio schemes with a unique hardware, and all the operating parameters even the functions of the radio system can be easily changed. This advantage is built on a solid hardware foundation. In other words, SDR system needs strong digital devices. In the past, the limited operating speed of ADC and processing ability of re-configurable chips for signal processing slowed down the development of SDR for useful commercial applications. This situation is changing with the rapid

development in semi-conductor processing technologies and re-configurable devices in combination with six-port receiver technology. With recent advances in the semi-conductor processing technology and the development of re-configurable devices such DSP and FPGA, SDR has now become practical for use in system solutions including wireless LANs, audio and television broadcasting and interoperability between different radio services.

As mentioned before, one of the advantages of SDR is that, it allows more efficient use of spectrum by facilitating spectrum sharing and by allowing equipment to be reprogrammed for various modulation schemes. Figure 2.1(a) shows the block diagram of a traditional narrow band digital receiver. In this kind of receiver, for each channel, there is an RF receiver and an IF receiver, RF receiver transfers signal from RF to IF and IF receiver transfers signal from IF to baseband. The baseband signals are digitalized and then sent to separate DSPs for signal processing.

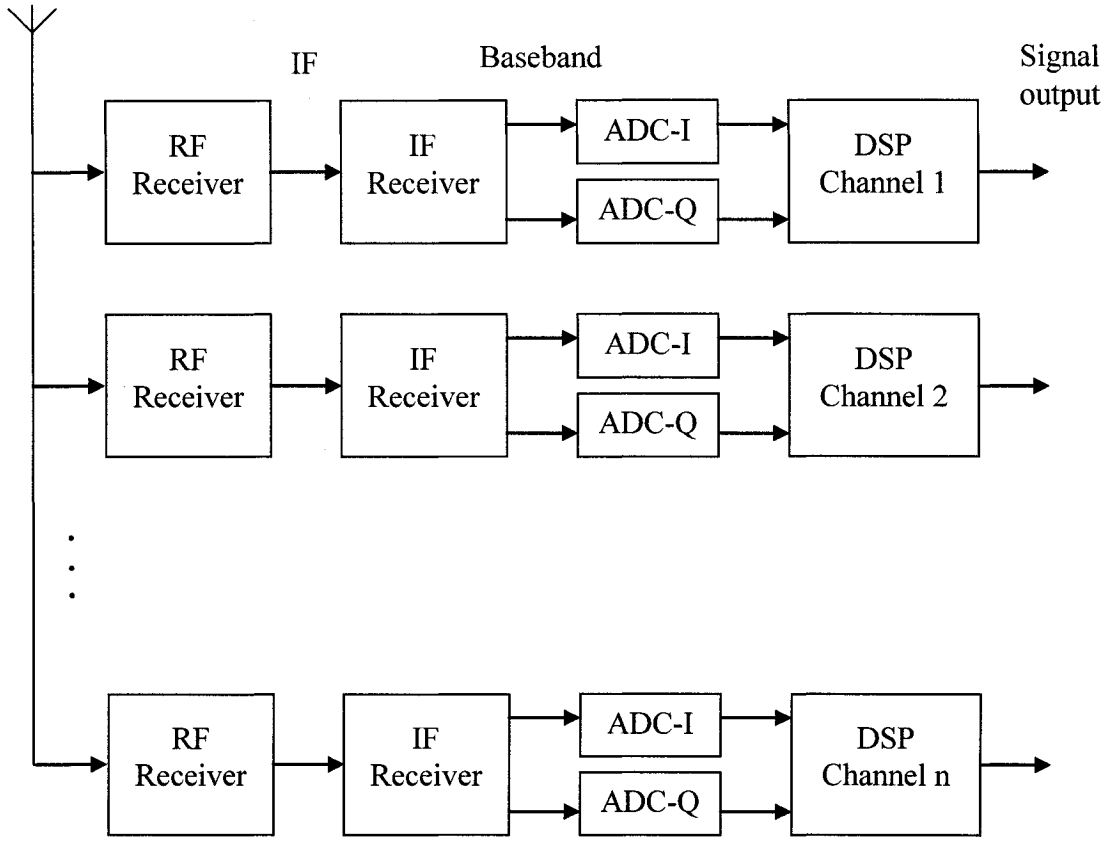


Figure 2.1 (a) Traditional narrow band digital receiver

Figure 2.1(b) shows the block diagram of a shared front-end SDR. There is only one wideband RF receiver for multi-channel. The received signals are sent to DSPs after being digitalized through the wideband ADC, and then the DSPs do channel selection and down-convert the digital signals from IF to baseband, if necessary, for signal processing. It can be seen that the radio front-end can be shared for multi-channel by software means. Therefore, the average cost of each channel is reduced.

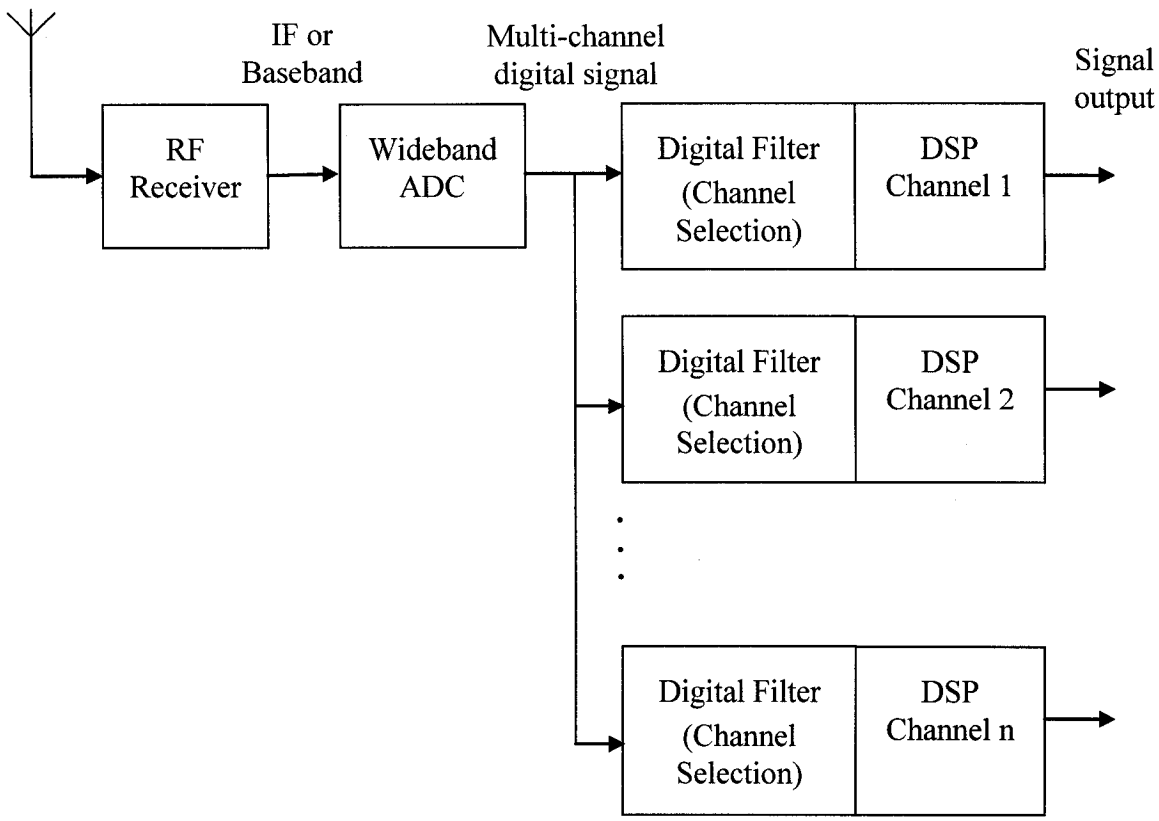


Figure 2.1(b) Software means for shared front-end of SDR receiver

2.3 Digital signal processing in Software Defined Radio

The old digital design paradigm for baseband and controller functions is based on single-stream instruction set processors optimized for high-speed arithmetic (DSP), hard-coded logic (ASIC), and single-stream instruction set processors optimized for message processing (microcontroller). Currently, the high-speed signal processing requirements for multi-mode multi-band are the most challenging. There are four major categories of new paradigm potential technical solutions [1], which are summarized in Table 2.1.

Table 2.1 Comparison of features of DSP, ASIC, parameterized hardware and FPGA

	Power consumption	Size	Cost	Field upgradeable	Silicon evolution	Tools
High-speed DSPs	Very high	Moderate	Moderate/ high	High	Easy	Some
Multiple ASICs	Moderate	Large	High	None	Difficult	Available
Parameterized hardware	Moderate	Moderate	Moderate	Some	Moderate	Some
FPGA	Low	Low	Moderate/ low	High	Easy	Available

High-speed instruction set processors to increase in speed, decrease in feature size, and improve at low-power operations. As these new generations of chips begin to appear and feature size continues to decline, there are proportionate increases in speed, power efficiency, and heat dissipation. However, for handheld system the high-speed processing requirements are still daunting. For example, if a particular algorithm requires 100 instructions to execute and the signal of interest is in the megahertz range, with memory access wait times and processor speed requirements, if performed entirely on a DSP, are in the gigahertz range. Gigahertz range clock speeds are likely to require power consumption and heat dissipation beyond the reach of current handsets.

Table 2.2 Comparison of FPGA and DSP chips

	FPGA chip	DSP chip
Programming language	VHDL, Verilog	C, Assembly Language
Ease of Software programming	Fairly easy, However, a programmer needs to understand the hardware architecture before programming.	Easy
Performance	Can be very fast if an appropriate architecture is designed	Speed is limited by the clock speed of a DSP chip
Reconfigurability	SRAM-type FPGAs can be reconfigurable an infinite number of times	Can be reconfiguration by changing program memory content
Reconfiguration method	Reconfiguration is done by download configuration data to a chip electronically	Reconfiguration is done by simply reading a program at a different memory address
Areas where FPGAs can outperform DSPs, or vice versa	FIR filter, IIR filter, correlator, convolver, FFT, etc.	A signal processing program of sequential nature
Power consumption	Can be minimized if the circuit is designed to save power, or the power is dynamically controlled.	Even if program A is larger than program B, power consumption does not change as long as the number of memory chips remains the same
Implementation method of MAC	Parallel multiplier/adder or distributed arithmetic	Repeated operation of MAC function
Speed of MAC	Can be fast if a parallel algorithm is used. If a filter is implemented using distributed arithmetic, the speed does not depend on the number of taps	Limited by the speed of MAC operation of a DSP chip. If a filter is implemented, the speed becomes slower if the number of taps increases
Parallelism	Can be parallelized to achieve high performance	DSP chip programming is usually sequential and cannot be parallelized

The use of reconfigurable logic such as FPGA for production implementations is the greatest departure from the DSP systems. An FPGA is an array of gates with programmable interconnect and logic functions that can be redefined after being manufactured. Field programmable devices can be grouped into the following two categories: programmable logic device (PLD) and FPGA. FPGA is more powerful and more popular than PLD. Generally, FPGA and DSP chips are the most popular used signal processing components in SDR systems. Table 2.2 shows the comparison between DSP and FPGA chips.

2.4 Combination of SDR and six-port technology

One key point of SDR is to possess a digital processing kernel with almost infinite processing ability. Although DSP and semiconductor technology have developed rapidly in the past ten years, the operating speed level of current DSP chips still can not completely support a high-speed multi-channel and multi-modulation SDR at IF level. In the interim, SDR implementations will require a mix of hardware-intensive techniques such as ASICs. Certain software radio systems adopt multi-chips architecture and parallel algorithms, thereby increasing the design complexity and potential cost.

Instead of digitalizing signals at IF, microwave/millimeter wave signals can also be digitalized at baseband with six-port technology, hence reducing the processing requirement for DSP chips. This new solution of SDR design is based on direct

demodulation with "six-port technology", down-converting RF signal to base-band directly by a six-port module. This dissertation presents works and results of the six-port receiver suitable for SDR which can be utilized in multi-mode multi-channel microwave/millimeter wave wireless mass-market communication systems. Detailed information of the six-port module is given in Chapter III below.

2.5 Broader Implications of the Software Radio

The prospect of a new technology for multi-band, multi-mode software radio-handsets and infrastructure has social and political implications particularly for type certification authorities charged with administering the equitable use of radio spectrum. Amongst other factors, these authorities certify that a radio equipment meets legally imposed constraints. The software radio introduces new levels of complexity in the communication hardware certification process.

In addition, software radios may operate on any RF band that is within the capabilities of the underlying radio platform, and with any mode for which a software load-image is available. This raises the possibility of truly novel approaches to spectrum management. One of the more interesting things is the possibility that software radios could use a spectrum rental protocol to autonomously share spectrum. Another is by incorporating advanced technology such as neural networks [21]-[23]. SDR can develop its own

protocols to achieve a radio system called "cognitive radios" [24]. Cognitive radio is an advanced research topic based on the software radio concept.

CHAPTER III

ARCHITECTURE AND OPERATING PRINCIPLE OF SIX-PORT RECEIVER

3.1 Introduction

Six-port technology has been under development during the past thirty years for microwave and millimeter wave measurement applications [19]. In 1994, Ji Li, R. G. Bosisio and Ke Wu proposed an application of this technology for direct receiver [2]. In principle, the circuitry of a six-port consists of dividers and combiners interconnected in such a way that four different sums of a reference signal and the signal to be measured are produced. Because of different lengths transmission lines between the components, the two signals generate different phase values at output ports, resulting in constructive or destructive interference. The signal levels of the four combined signals are detected using Schottky diode detectors. By applying suitable algorithms, the magnitudes and phases of the unknown RF signal can be determined for any given modulation scheme [9], [25] from the four power values and calibration coefficients obtained from physical calibration [26] or regenerative data calibration [27].

3.2 Architecture of six-port SDR receiver

The structure of a software six-port receiver is shown in Figure 3.1. A six-port circuit works as an RF down-converter in the proposed receiver. Two input ports of the six-port connect to RF signal and LO respectively, and the other four output ports are connected to power detectors. Signals from two input ports are directly down-converted from RF to baseband frequency in the form of the output of the power detectors. The signals from power detectors are digitalized and sent to the DSP stage. The DSP stage is in charge of baseband signal processing such as demodulation and decoding. The receiver is designed to operate at millimeter wave frequency and operate over a wideband (22-26 GHz) for multi-mode schemes.

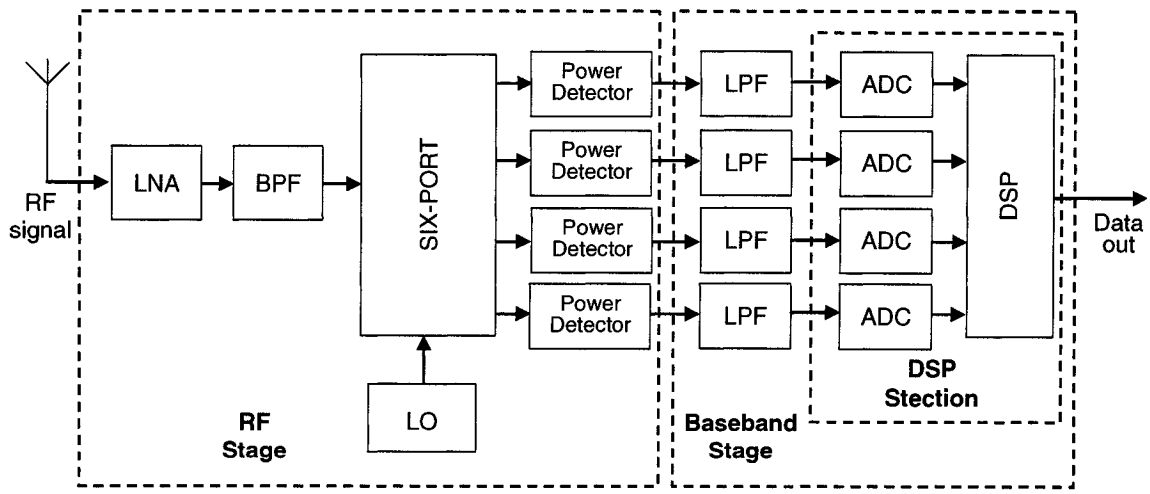


Figure 3.1 Architecture of six-port SDR receiver

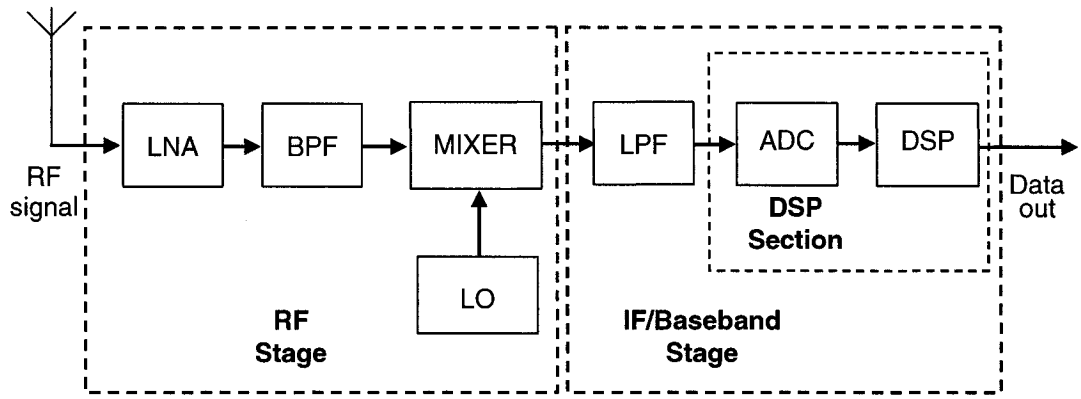


Figure 3.2 Block diagram of traditional SDR receiver (without six-port)

The block diagram of typical practical SDR receiver is shown in Figure 3.2. Limited by the operating speed capability of current DSP chips, the radio frequency signals are down-converted to IF or baseband frequency before been digitized and sent to the DSP.

Comparing with traditional SDR receiver system in Figure 3.2, the six-port SDR receiver has wider bandwidth, lower cost for RF front-end circuits and lower DSP capability requirement. For certain modulation schemes (e.g. QPSK), there are fast demodulation algorithms for six-port receiver that make the DSP demodulation code very simple.

As mentioned in Chapter I, the six-port receiver approach offers wide band accommodation to ever-changing communication specifications required in an SDR. Some six-ports offer wide bandwidth from 2-2200 MHz [10], 0.5-9 GHz and 22-31 GHz [11]. Therefore, the six-port receiver can be used in various applications such as FM

radio, TV, cordless phones, paging, global positioning system (GPS), digital audio broadcasting (DAB), mobile satellite (MSAT), personal communication service (PCS), radar satellite, satellite multimedia, local multipoint communication systems (LMCS), ultra-wide band (UWB) communication and so on.

As we know, wideband down-converters are not readily available at millimeter wave frequencies. In a six-port SDR receiver, six-port circuit plus power detectors work as a down-converter, which offers a cost-effective approach to directly down-convert RF signal to baseband signal. In addition, the relative low frequency baseband signals reduce the ADCs sampling and DSP capability requirement. On the other hand, the six-port receiver needs a set of 4 BPF and ADCs, which potentially increase the system cost; however, with the recent development of ASIC technology, the price of these components will be significantly reduced.

3.3 Operating principle of six-port reflectometer

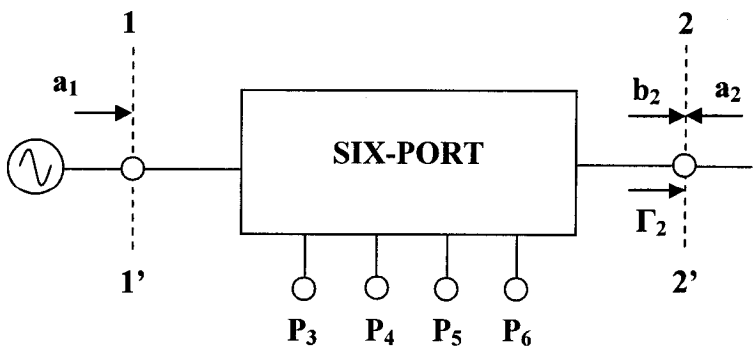


Figure 3.3 Block diagram of six-port reflectometer

The structure of a conventional six-port is shown in Figure 3.3. To achieve accurate measurment results, a calibration procedure is needed. Calibration coefficients of the six-port are obtained by regenerative means or physical standards. Connect port 2 to RF signal, port 1 to reference signal and the other four ports to power detectors, the complex ratio of the two input signals a_1 and a_2 in Figure 3.3 can be obtained as follows:

$$\frac{\vec{a}_1}{\vec{a}_2} = \frac{\sum_{i=3}^{6}(a_i + jb_i)P_i}{\sum_{i=3}^{6}(c_i + jd_i)P_i} \tag{3.1}$$

where constants a_i, b_i, c_i, d_i are calibration parameters that depict the specific six-port and can be calculated from the two-step calibration procedure which is shown below.

The response of the six-port can be obtained from four power level readings:

$$P_3 = |b_3|^2 = |Aa_2 + Bb_2|^2 \tag{3.2}$$

$$P_4 = |b_4|^2 = |Ca_2 + Db_2|^2 \tag{3.3}$$

$$P_5 = |b_5|^2 = |Ea_2 + Fb_2|^2 \tag{3.4}$$

$$P_6 = |b_6|^2 = |Ga_2 + Hb_2|^2 \tag{3.5}$$

where $A \ldots H$ are complex constants, presumed to be known by calibration procedures,

$$|b_2|^2 = \sum_{i=3}^{6} \beta_i P_i$$

and β_i are real coefficients, functions of $A \ldots H$.

The measurement of $|b_2|$ represents a determination of one of the measurement of interest. The six-port is usually designed in such a way that the response of one of the power detectors is proportional to $|b_2|^2$. The 4th port is chosen for normalization. Referring to equation (3.3), the first design objective is for $C = 0$

Hence

$$P_4 = |D|^2 |b_2|^2 \tag{3.6}$$

In order to explicitly display the measurements of interest, (3.2), (3.4) and (3.5) may be written as,

$$P_3 = |A|^2 |b_2|^2 |\Gamma_2 - q_3|^2 \tag{3.7}$$

$$P_5 = |E|^2 |b_2|^2 |\Gamma_2 - q_5|^2 \tag{3.8}$$

$$P_6 = |G|^2 |b_2|^2 |\Gamma_2 - q_6|^2 \tag{3.9}$$

where $q_3 = -B/A$, $q_5 = -F/E$, $q_6 = -H/G$.

Since A, E, G can be known by calibration procedures, $|b_2|$ and Γ_2 can be determined from equation (3.6) ~ (3.9). First, $|b_2|^2$ can be eliminated from equation (3.7), equation (3.8) and equation (3.9) by means of equation (3.6). That leads to:

$$|\Gamma_2 - q_3|^2 = \left|\frac{D}{A}\right|^2 \cdot \frac{P_3}{P_4} \tag{3.10}$$

$$|\Gamma_2 - q_5|^2 = \left|\frac{D}{E}\right|^2 \cdot \frac{P_5}{P_4} \tag{3.11}$$

$$|\Gamma_2 - q_6|^2 = \left|\frac{D}{G}\right|^2 \cdot \frac{P_6}{P_4} \tag{3.12}$$

From equation (3.10), the locus of possible values for Γ_2 is a circle with center at q_3 and whose radius is $|\Gamma_2 - q_3|^2$. In the same way, from equation (3.11) and equation (3.12), two other circles which contain Γ_2 can be determined. With centers at q_5 and q_6, their radius are $|\Gamma_2 - q_5|^2$ and $|\Gamma_2 - q_6|^2$, respectively. The situation is shown in Figure 3.4. Here Γ_2 is determined by the intersection of the three circles. In practice, due to measurement errors, the three circles may not intersect in a point, and some sort of statistical weighting is called for.

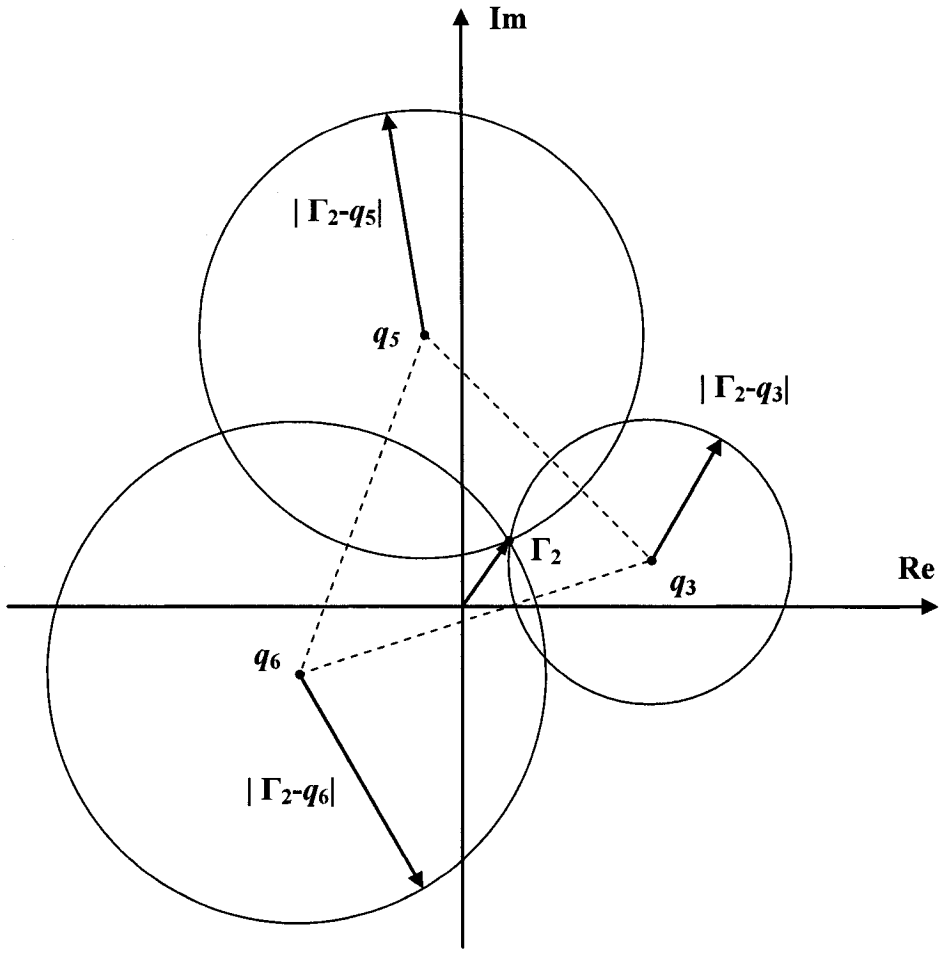


Figure 3.4 Determination of Γ_2 from the intersection of three circles

Consider the case at reference plan 2-2' in Figure 3.3. The "incident wave" a_2 and the "reflect wave" b_2 are in frequency f_{RF}, f_{LO} and have arbitrary relative relationships φ_1, φ_2. So that,

$$a_2 = | a | e^{j(2\pi f_{RF} t + \varphi_1)} \tag{3.13}$$

$$b_2 = |b| e^{j(2\pi f_{LO} t + \varphi_2)} \tag{3.14}$$

If their frequency difference between a_2 and b_2 is small, the S-parameters of the six-port to be calibrated can be regarded as being constant at each frequency and the equivalent reflection coefficient becomes:

$$\Gamma_2 = \frac{b_2}{a_2} = \left|\frac{b}{a}\right| e^{j(2\pi \Delta f t + \Delta\varphi)} \tag{3.15}$$

where, $\Delta f = f_{LO} - f_{RF}$ and $\Delta\varphi = \varphi_2 - \varphi_1$

The frequency difference Δf can be readily obtained from the derivative of $\theta(t)$

$$\Delta f = \frac{\theta(t_2) - \theta(t_1)}{t_2 - t_1} \tag{3.16}$$

where the time interval between two samples $\Delta t = t_2 - t_1$ is properly chosen for best accuracy. It is to be noted that the sign of Δf is a direct indication of the relative position of f_{RF} and f_{LO}. In this way, we can then know the ratio of amplitude, frequency and phase between the LO signal (port 1) and the RF signal (port 2) from the power output at the other four ports. Thus,

$$\Gamma_2 = \frac{\sum_{i=3}^{6} X_i P_i}{\sum_{i=3}^{6} Y_i P_i} \tag{3.17}$$

where X_i, Y_i are complex constants which could be obtained from calibration procedures.

By a simple approach, the six-port system may be expended to seven or more ports. In this way, Γ_2 could be determined from the intersection of four or more circles. However, the additional complexity does not ordinarily warrant the accuracy improvement.

3.4 Analysis of six-port circuit

One of the design criteria for an ideal six-port junction as suggested by Engen [28] are as follows:

For the ideal situation, a six-port circuit can obtain the highest accuracy for all ranges of device under test (DUT) if the q points correspond to the following conditions:

- C=0 [see equation (3.3)]
- $|q_3| = |q_5| = |q_6|$ and their arguments differ by $\pm 120°$

Suppose port 1 and port 2 are isolated, the equivalent q_i point can be expressed as

$$q_i = \frac{S_{i1}}{S_{i2}} \tag{3.18}$$

In a practical situation, it is difficult to find such a circuit especially if broad band operation is required. In general, the more equal the magnitudes of q_i and the bigger the differences of arguments of q_i, the better the performance of the circuit. According to [29], the six-port can yield good results even when the ratios of the magnitudes of q_i are bigger than 4 and the angles between q_i are smaller than 25°.

Some six-port junction models are shown in Figure 3.5. All these six-port junctions consist of power dividers, hybrid couplers and phase shifters. In Figure 3.5 "P" represents a power divider and "Q" represents a 90-degree 3-db hybrid coupler.

Figure 3.5(a) is a six-port junction combined with one power divider and three 90-degree 3-db hybrid couplers. This model was proposed as a typical six-port model for microwave and millimeter wave measurement applications and was adopted by six-port receiver design [9] for the first time (discussed in Chapter IV below).

Figure 3.5(b) is a real "six-port" with two power dividers, two 90-degree 3-db hybrid couplers and one 90-degree phase shifter. This model is used in the novel SIW six-port (discussed in Chapter V below) for SDR receiver platform.

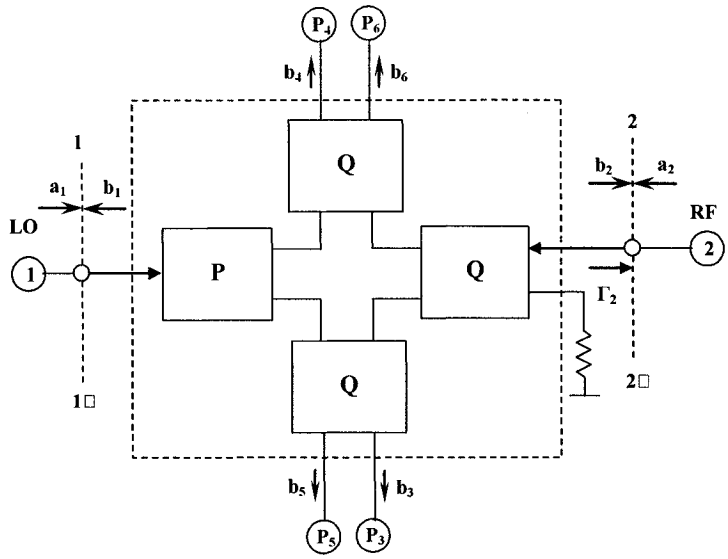


Figure 3.5 (a) Six-port junction model 1

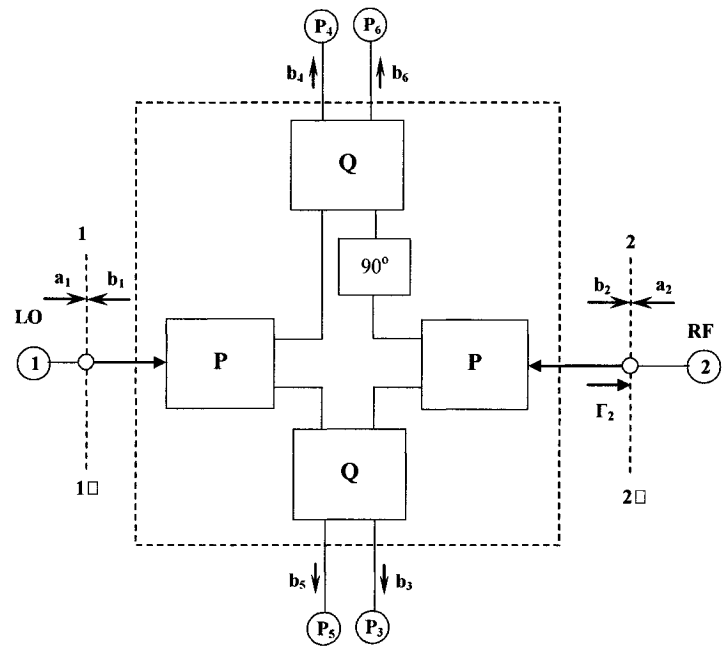


Figure 3.5 (b) Six-port junction model 2

Figure 3.5(c) is an eight-port circuit combined with four 90-degree 3-db hybrid couplers and one 90-degree phase shifter. Two extra ports are connected with 50 Ohm terminals. This model has been adopted in new collision avoidance radar sensor applications [30].

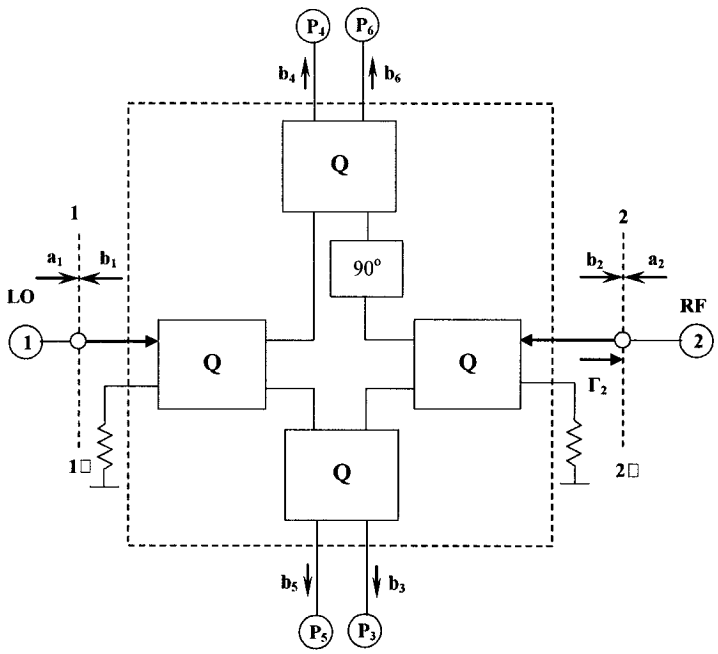
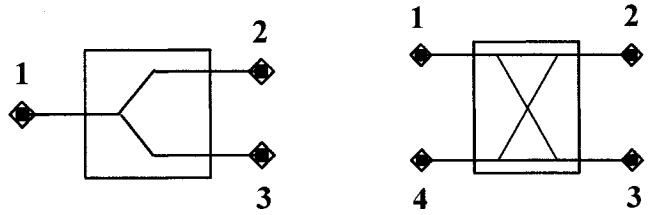


Figure 3.5 (c) Six-port junction model 3

All the six-port junctions presented here consist of power dividers and 90-degree 3-db hybrid couplers. Figure 3.6 shows the symbols and the scattering parameters of these two components. We choose the Wilkinson power divider as representation of an ideal power divider.



(a) (b)

Figure 3.6 (a) Power divider (b) 90-degree 3-db hybrid coupler

Wilkinson power divider:
$$[S]=\begin{bmatrix} 0 & -\frac{j}{\sqrt{2}} & -\frac{j}{\sqrt{2}} \\ -\frac{j}{\sqrt{2}} & 0 & -\frac{j}{\sqrt{2}} \\ -\frac{j}{\sqrt{2}} & -\frac{j}{\sqrt{2}} & 0 \end{bmatrix} \tag{3.19}$$

90-degree 3-db hybrid coupler:
$$[S]=\begin{bmatrix} 0 & -\frac{j}{\sqrt{2}} & -\frac{1}{\sqrt{2}} & 0 \\ -\frac{j}{\sqrt{2}} & 0 & 0 & -\frac{1}{\sqrt{2}} \\ -\frac{1}{\sqrt{2}} & 0 & 0 & -\frac{j}{\sqrt{2}} \\ 0 & -\frac{1}{\sqrt{2}} & -\frac{j}{\sqrt{2}} & 0 \end{bmatrix} \tag{3.20}$$

Now we consider the scattering parameters of these three virtual six-ports. For model 1 which is shown in Figure 3.5(a), assume that all the 6 ports are perfectly matched, so $S_{11} = S_{22} = S_{33} = S_{44} = S_{55} = S_{66} = 0$. From (3.19) and (3.20), the reflected waves at port 1 to port 6 can be expressed as:

$$
\begin{aligned}
b_1 &= 0 \\
b_2 &= 0 \\
b_3 &= \frac{a_1}{2} j + \frac{a_2}{2} j \\
b_4 &= -\frac{a_1}{2} + \frac{a_2}{2} j \\
b_5 &= -\frac{a_1}{2} + \frac{a_2}{2} \\
b_6 &= \frac{a_1}{2} j - \frac{a_2}{2}
\end{aligned}
\tag{3.21}
$$

Since

$$
[b] = [S] \cdot [a] \tag{3.22}
$$

We can list the scattering parameters for six-port model 1 as follows:

$$
\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \\ b_5 \\ b_6 \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{1}{2}e^{j90^\circ} & \frac{1}{2}e^{j180^\circ} & \frac{1}{2}e^{j180^\circ} & \frac{1}{2}e^{j90^\circ} \\ 0 & 0 & \frac{1}{2}e^{j90^\circ} & \frac{1}{2}e^{j90^\circ} & \frac{1}{2}e^{j0^\circ} & \frac{1}{2}e^{j180^\circ} \\ \frac{1}{2}e^{j90^\circ} & \frac{1}{2}e^{j90^\circ} & 0 & 0 & 0 & 0 \\ \frac{1}{2}e^{j180^\circ} & \frac{1}{2}e^{j90^\circ} & 0 & 0 & 0 & 0 \\ \frac{1}{2}e^{j180^\circ} & \frac{1}{2}e^{j0^\circ} & 0 & 0 & 0 & 0 \\ \frac{1}{2}e^{j90^\circ} & \frac{1}{2}e^{j180^\circ} & 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \\ a_5 \\ a_6 \end{bmatrix} \tag{3.23}
$$

The S-parameters of model 2 and model 3 can be calculated the way same as we do with model 1.

For model 2:

$$
\begin{aligned}
b_1 &= 0 \\
b_2 &= 0 \\
b_3 &= \frac{a_1}{2} j - \frac{a_2}{2} \\
b_4 &= -\frac{a_1}{2} + \frac{a_2}{2} \\
b_5 &= -\frac{a_1}{2} + \frac{a_2}{2} j \\
b_6 &= \frac{a_1}{2} j + \frac{a_2}{2} j
\end{aligned}
\tag{3.24}
$$

$$
\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \\ b_5 \\ b_6 \end{bmatrix} =
\begin{bmatrix}
0 & 0 & \frac{1}{2}e^{j90^\circ} & \frac{1}{2}e^{j180^\circ} & \frac{1}{2}e^{j180^\circ} & \frac{1}{2}e^{j90^\circ} \\
0 & 0 & \frac{1}{2}e^{j180^\circ} & \frac{1}{2}e^{j0^\circ} & \frac{1}{2}e^{j90^\circ} & \frac{1}{2}e^{j90^\circ} \\
\frac{1}{2}e^{j90^\circ} & \frac{1}{2}e^{j180^\circ} & 0 & 0 & 0 & 0 \\
\frac{1}{2}e^{j180^\circ} & \frac{1}{2}e^{j0^\circ} & 0 & 0 & 0 & 0 \\
\frac{1}{2}e^{j180^\circ} & \frac{1}{2}e^{j90^\circ} & 0 & 0 & 0 & 0 \\
\frac{1}{2}e^{j90^\circ} & \frac{1}{2}e^{j90^\circ} & 0 & 0 & 0 & 0
\end{bmatrix} \cdot
\begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \\ a_5 \\ a_6 \end{bmatrix}
\tag{3.25}
$$

For model 3:

$$
\begin{aligned}
b_1 &= 0 \\
b_2 &= 0 \\
b_3 &= \frac{a_1}{2} + \frac{a_2}{2} j \\
b_4 &= -\frac{a_1}{2} + \frac{a_2}{2} \\
b_5 &= \frac{a_1}{2} j + \frac{a_2}{2} \\
b_6 &= \frac{a_1}{2} j + \frac{a_2}{2} j
\end{aligned}
\tag{3.26}
$$

$$
\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \\ b_5 \\ b_6 \end{bmatrix} =
\begin{bmatrix}
0 & 0 & \frac{1}{2}e^{j0^\circ} & \frac{1}{2}e^{j180^\circ} & \frac{1}{2}e^{j90^\circ} & \frac{1}{2}e^{j90^\circ} \\
0 & 0 & \frac{1}{2}e^{j90^\circ} & \frac{1}{2}e^{j0^\circ} & \frac{1}{2}e^{j0^\circ} & \frac{1}{2}e^{j90^\circ} \\
\frac{1}{2}e^{j0^\circ} & \frac{1}{2}e^{j90^\circ} & 0 & 0 & 0 & 0 \\
\frac{1}{2}e^{j180^\circ} & \frac{1}{2}e^{j0^\circ} & 0 & 0 & 0 & 0 \\
\frac{1}{2}e^{j90^\circ} & \frac{1}{2}e^{j0^\circ} & 0 & 0 & 0 & 0 \\
\frac{1}{2}e^{j90^\circ} & \frac{1}{2}e^{j90^\circ} & 0 & 0 & 0 & 0
\end{bmatrix} \cdot
\begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \\ a_5 \\ a_6 \end{bmatrix}
\tag{3.27}
$$

where a_1 and a_2 represent the reference (LO) signal and the incoming RF signal, respectively.

CHAPTER IV

MHMIC MICROSTRIP SIX-PORT CIRCUIT DESIGN

4.1 Introduction

Based on the analysis of the ideal six-port junction in Chapter III, a microstrip six-port circuit is designed. The objective is to design a six-port circuit for SDR receiver at a center frequency of 24 GHz. Because six-port receiver requires good stability and high sensitivity, this leads to the following design criteria:

- Minimized insertion loss between the RF input port and power detector ports to increase sensitivity.
- Maximized isolation between the RF input port and LO port to reduce leakage to the antenna.
- The q_i points should be equal in magnitude and 120° different from each other in phase. Suppose the RF input port and LO port are isolated, the equivalent q_i points can be expressed as, $q_3 = \frac{S_{31}}{S_{32}}$, $q_5 = \frac{S_{51}}{S_{52}}$, $q_6 = \frac{S_{61}}{S_{62}}$.
- Maximized temperature stability.

Using the software Advanced Design System (ADS) of Agilent Technologies, a microstrip six-port circuit has been designed and fabricated at the centre frequency of 24

GHz with the bandwidth from 22 GHz to 26 GHz. The six-port circuit consists of a Wilkinson coupler (work as a power divider) and three quadrature hybrid couplers. The simulated S-parameters of the designed Wilkinson coupler and quadrature hybrid couplers are presented in sections 4.2 and 4.3. Referring to S. O. Tatu's 27 GHz six-port circuit design [11], the proposed six-port circuit is fabricated in MHMIC technology on a 0.254 mm ceramic substrate with a relative permittivity $\varepsilon_r = 9.9$. The MHMIC chip measures 9.5x8.4 mm. The corresponding wavelength at centre frequency is 4.73 mm. The simulated and measured S-parameters of the proposed microstrip six-port circuit are given in sections 4.4 and 4.5, respectively.

4.2 Wilkinson Coupler

A Wilkinson coupler is used in the proposed six-port circuit. It divides the signal from LO into two signals with equal amplitude and phase. The microstrip implementation of 3-dB Wilkinson coupler is shown in Figure 4.1 (a) and the microstrip layout of the designed 3-dB Wilkinson coupler is shown in Figure 4.1(b) in which $Z_0 = 50$ Ohm and $Z_{01} = 70.7$ Ohm. It is a three-port network that divides equally the input power at port 1 to port 2 and port 3 when the ports are terminated in $Z_0 = 50$ Ohm. The signals at ports 2 and 3 are of equal amplitude and phase.

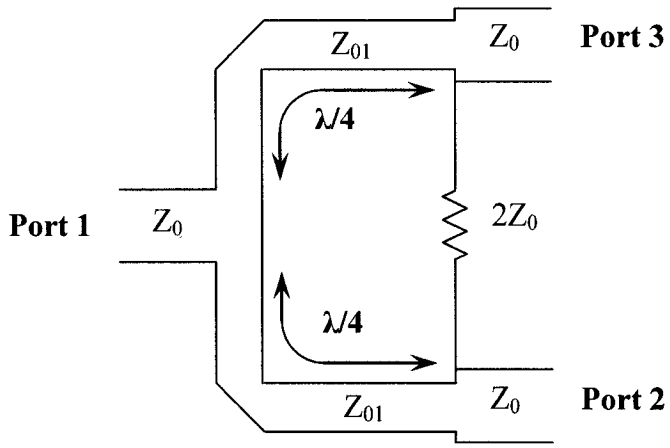


Figure 4.1 (a) Microstrip implementation of a Wilkinson coupler

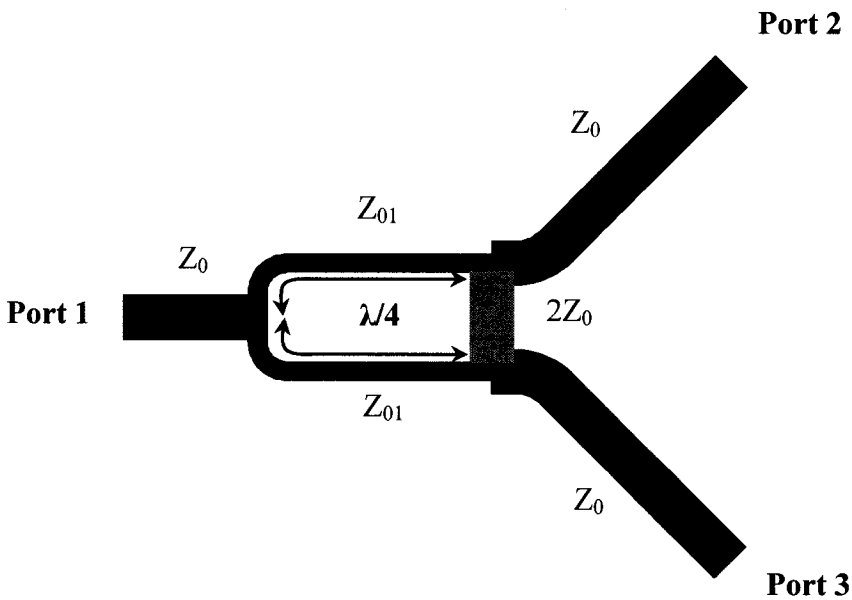


Figure 4.1(b) Layout microstrip Wilkinson coupler

The operating principle of the Wilkinson coupler is that each λ/4 line transforms the 50 Ohm termination to an input impedance of 100 Ohm. Then port 1 sees 100 Ohm in parallel with 100 Ohm, which produces the desired 50 Ohm input impedance. Therefore, when port 2 and 3 are terminated in 50 Ohm, the input port 1 should see an input impedance of 50 Ohm, that is to say, the input port 1 is matched. The transformation of 50 Ohm to 100 Ohm by λ/4 line is accomplished by selecting its characteristic impedance as $Z_{01} = \sqrt{100(50)} = 70.7\Omega$. No power is dissipated in the 100 Ohm resistor connected between port 2 and 3 when equal loads are connected to port 2 and 3.

When a mismatch occurs at an output port (e.g., at port 2), a reflected signal is generated which splits between the transmission line and the 100 Ohm resistor. These two signals appear at port 3 with a 180^{o} phase shift, and cancellation occurs. The value of the resistor was selected so that the two parts of the reflected signal have equal amplitude and, therefore, perfect cancellation results. Similar considerations apply if a mismatch occurs at port 3.

To test the performance of the designed Wilkinson coupler, an S-parameters simulation is made using ADS at center frequency f_0 = 24 GHz. The simulated S-parameters curves are shown in Figure 4.2 and the comparison between simulated values and theoretic values are listed in Table 4.1.

Table 4.1 S-parameters of the Wilkinson coupler

S-parameters	Theoretic		Simulated	
	Magnitude	Phase	Magnitude	Phase
S_{11}	0	0	0.003 (-50.1 dB)	-66.6
S_{22}	0	0	0.015 (-36.6 dB)	-97.9
S_{33}	0	0	0.017 (-35.2 dB)	111.4
$S_{12}=S_{21}$	0.707 (-3 dB)	-90	0.692 (-3.195 dB)	-92.6
$S_{13}=S_{31}$	0.707 (-3 dB)	-90	0.692 (-3.195 dB)	-92.6
$S_{23}=S_{32}$	0	0	0.017 (-35.2 dB)	111.4

It can be seen from the simulated result that all the three ports of the designed Wilkinson coupler are matched (S_{11}, S_{22}, S_{33} are less than -35 dB). Port 2 and port 3 are isolated (S_{32} is less than -35 dB), and the transmission parameters (S_{12}, S_{13}) are very close to the theoretical values 0.707 (-3dB).

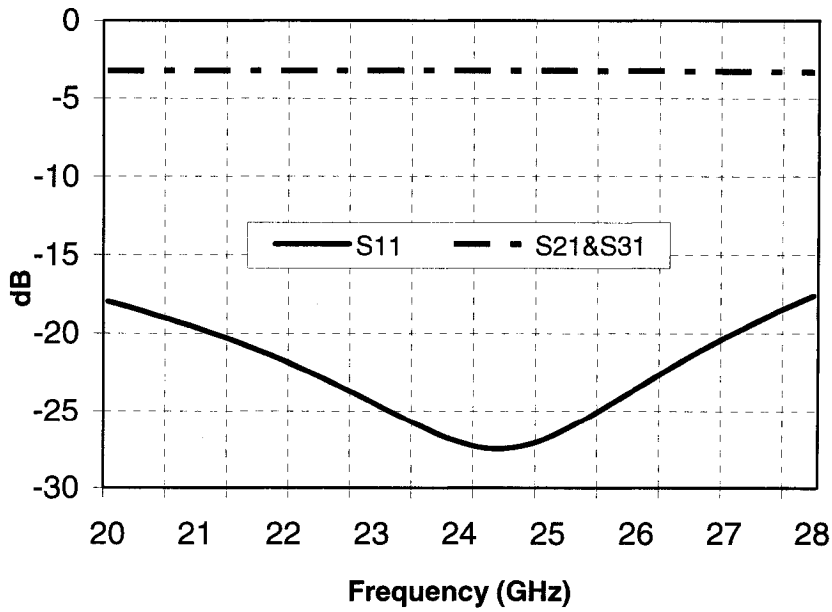


Figure 4.2 Simulated S-parameters of the designed Wilkinson coupler

4.3 Quadrature Hybrid coupler

Three 90-degree hybrid couplers are used in the proposed microstrip six-port circuit. It provides two output signals with 90-degree phase difference. A microstrip implementation of a quadrature hybrid coupler is shown in Figure 4.3 (a) and the microstrip layout of the designed quadrature hybrid coupler is shown in Figure 4.3 (b), in which Z_0 = 50 Ohm and Z_{02} = 35.4 Ohm.

In Figure 4.3, with 50 Ohm terminations at ports 2, 3 and 4, the input power at port 1 divides equally between ports 2 and port 3, with zero power at port 4. Specifically, the operating principle of the coupler is as follow. With an input source of 50 Ohm impedance applied to port 1, and with ports 2, 3, and 4 terminated in 50 Ohm, the incident wave a_1 at port 1 appears as $a_1 e^{-j\pi/2}/\sqrt{2}$ at port 2 and as $a_1 e^{-j\pi}/\sqrt{2}$ at port 3. Port 1 sees a matched input impedance, and the phase shift between ports 2 and 3 is $\pi/2$. From the symmetry of the coupler, it also follows that after exciting port 2, the signal power divides and couples to ports 1 and 4; exciting port 3, the signal power divides and couples to ports 4 and 1; and exciting port 4, the signal power divides and couples to ports 3 and 2. The driven port sees as matched impedance when the other ports are terminated in their matched impedance.

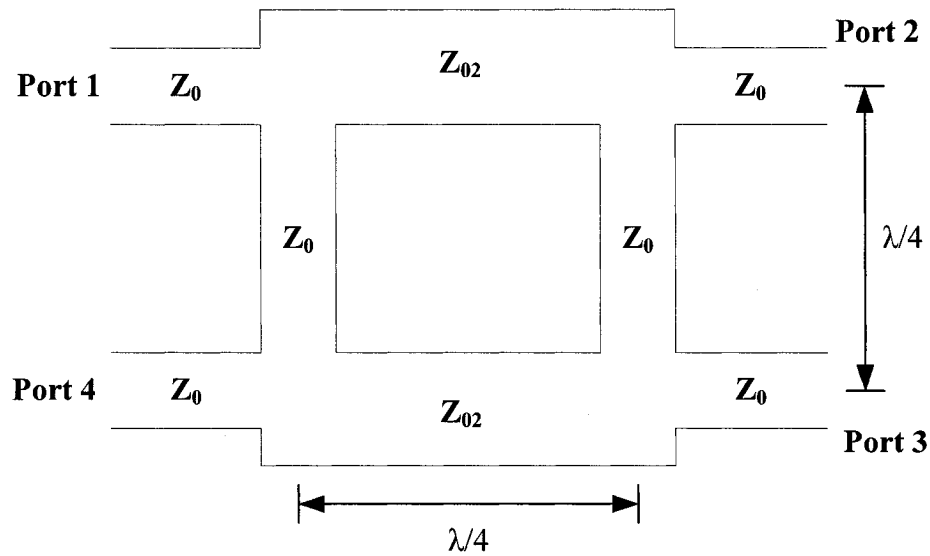


Figure 4.3 (a) Microstrip implementation of a microstrip 3-dB quadrature hybrid coupler

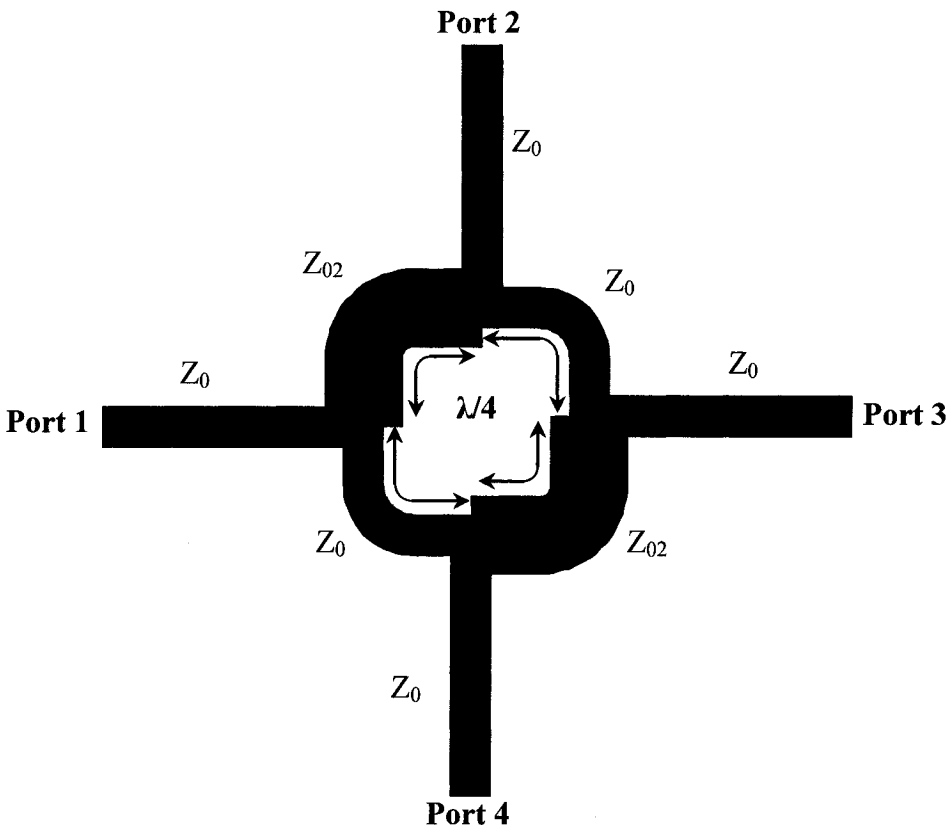


Figure 4.3 (b) Microstrip layout of 3-dB quadrature hybrid coupler

S-parameters simulation of the quadrature hybrid coupler is made using ADS at center frequency f_0 = 24 GHz. The simulated S-parameters curves are shown in Figure 4.4 and the comparison between simulated and theoretic S-parameters values are listed in Table 4.2.

Table 4.2 S-parameters of the quadrature hybrid coupler

S-parameters	Theoretic		Simulation	
	Magnitude	Phase (deg)	Magnitude	Phase (deg)
S_{11}	0	0	0.055 (-25.3dB)	-164.7
S_{22}	0	0	0.055 (-25.3dB)	-164.7
S_{33}	0	0	0.055 (-25.3dB)	-164.7
S_{44}	0	0	0.055 (-25.3dB)	-164.7
$S_{14} = S_{41}$	0	0	0.046 (-26.8dB)	68.7
$S_{23} = S_{32}$	0	0	0.046 (-26.8dB)	68.7
$S_{12} = S_{21}$	0,707 (-3dB)	-90	0.708 (-3.0dB)	-91.3
$S_{13} = S_{31}$	0,707 (-3dB)	-180	0.672 (-3.45dB)	-181.0
$S_{42} = S_{24}$	0,707 (-3dB)	-180	0.672 (-3.45dB)	-181.0
$S_{43} = S_{34}$	0,707 (-3dB)	-90	0.708 (-3.0dB)	-91.3

It can be seen from the simulated results that all the four ports of the designed quadrature coupler are matched (S_{11}, S_{22}, S_{33} S_{44} are less than -25 dB). Port 1, 4 and port 2, 3 are isolated (S_{14} and S_{32} is less than -26 dB), and the transmission parameters (S_{12}, S_{13}, S_{42}, S_{43}) are close to the theoretical values 0.707 (-3dB) while the phases of the two output signals have 90 degree difference.

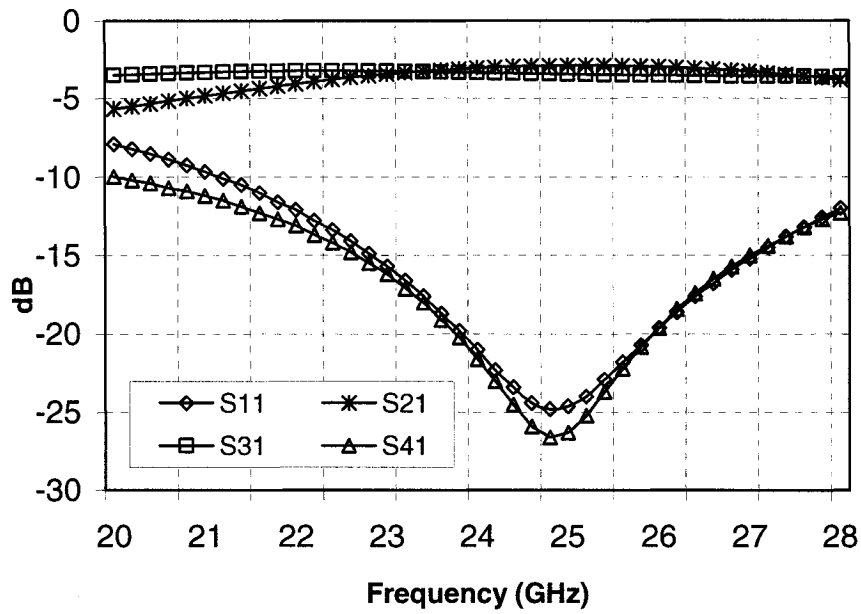


Figure 4.4 Simulated S-parameters of the designed quadrature hybrid coupler

4.4 Simulation of the six-port circuit

The microstrip layout of the proposed six-port circuit is shown in Figure 4.5. As indicated in Figure 3.3 (a), this six-port circuit combines one Wilkinson power divider and three 3-db quadrature hybrid couplers. In a six-port receiver, port 1 and port 2 are input ports and port 3, 4, 5, 6 are output ports. Port 1 connects to the LO as reference signal; port 2 connects to the received RF signal from the antenna. Ports 3, 4, 5, 6 connect to power detectors. The six-port circuit measures 9.5 × 8.4 mm.

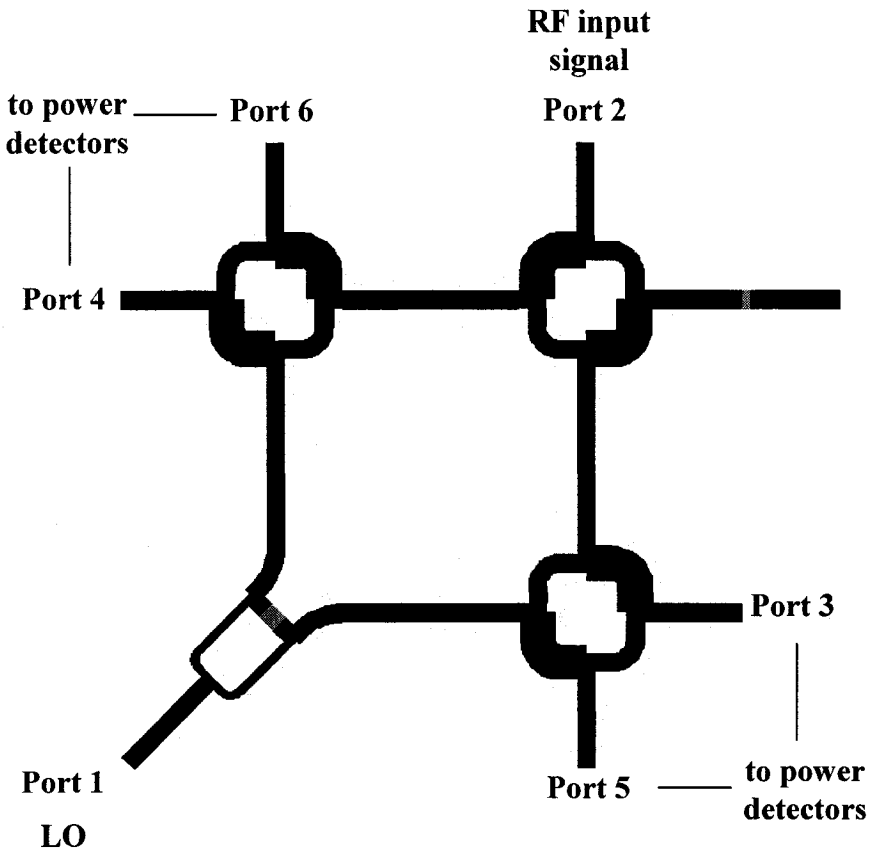


Figure 4.5 Design layout of the six-port circuit

S-parameters simulation of the proposed six-port circuit is made using ADS at center frequency f_0 = 24 GHz, and the comparison between simulated values and theoretic values are listed in Table 4.3.

It can be seen from Table 4.3 that the proposed six-port circuit has very good match (S_{11}, S_{22}, S_{33}, S_{44}, S_{55}, S_{66} are less than -20dB) and isolation (S_{12}, S_{34}, S_{35}, S_{36}, S_{45}, S_{46}, S_{56} are less than -20dB). While the transfer parameters (S_{31}, S_{41}, S_{51}, S_{61}, S_{32}, S_{42}, S_{52}, S_{62}) are very close to the theoretical values.

Table 4.3 Simulated S-parameters of the six-port circuit

S-parameters	Theoretic		Simulated	
	Magnitude	Phase (deg)	Magnitude	Phase (deg)
S_{11}	0	0	0.012 (-38.3dB)	96.5
S_{22}	0	0	0.021 (-33.7dB)	171.3
S_{33}	0	0	0.093 (-20.7dB)	128.3
S_{44}	0	0	0.086 (-21.3dB)	116.8
S_{55}	0	0	0.069 (-23.2dB)	-75.7
S_{66}	0	0	0.071 (-23.0dB)	-91.81
S_{12}	0	0	0.009 (-40.6dB)	-118.7
S_{31}	0.5 (-6 dB)	90	0.471 (-6.5dB)	90.1
S_{41}	0.5 (-6 dB)	180	0.468 (-6.6dB)	179.9
S_{51}	0.5 (-6 dB)	180	0.469 (-6.6dB)	179.7
S_{61}	0.5 (-6 dB)	90	0.472 (-6.5dB)	90.0
S_{32}	0.5 (-6 dB)	90	0.479 (-6.4dB)	90.2
S_{42}	0.5 (-6 dB)	90	0.478 (-6.4dB)	89.9
S_{52}	0.5 (-6 dB)	0	0.481 (-6.4dB)	0.247
S_{62}	0.5 (-6 dB)	180	0.477 (-6.4dB)	179.8
S_{34}	0	0	0.069 (-23.3dB)	-68.2
S_{35}	0	0	0.068 (-23.4dB)	10.3
S_{36}	0	0	0.086 (-21.4dB)	11.5
S_{45}	0	0	0.086 (-21.3dB)	-168.3
S_{46}	0	0	0.089 (-21.0dB)	-150.6
S_{56}	0	0	0.069 (-23.3dB)	-68.1

The proposed MHMIC microstrip six-port circuit is designed at center frequency 24 GHz with 4 GHz (22-26GHz) bandwidth. The simulated S-parameters of the proposed six-port circuit are shown in Figure 4.6 ~ Figure 4.13.

Figure 4.6 shows the return loss (S_{11}, S_{22}) and the isolation (S_{12}) of the two input ports (port 1 and port 2) within the operating bandwidth. From the figure, it can be found that the return loss of port 1 and port 2 are lower than -30 dB at center frequency (24 GHz) and are lower than -20 dB for most of the operation bandwidth. The isolation between the two input ports is -60 dB at center frequency and is lower than -20 db for almost all the frequency band.

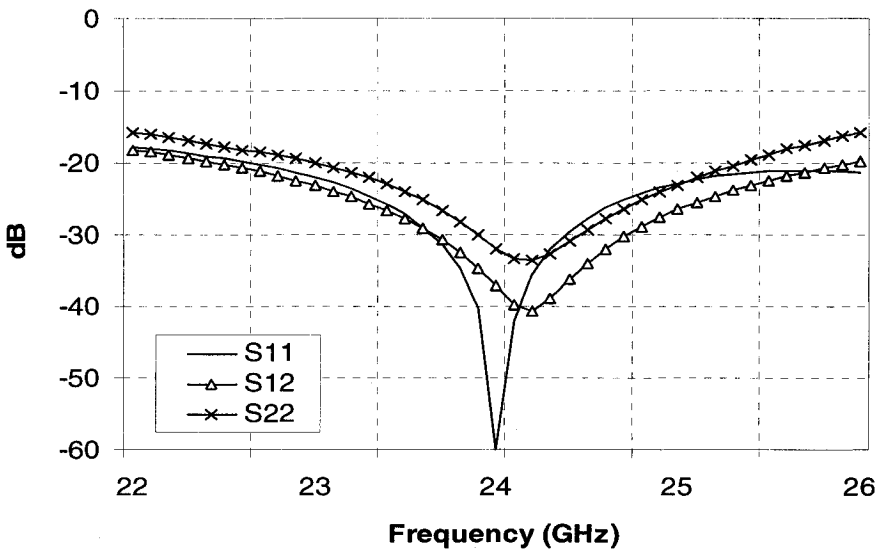


Figure 4.6 Simulated return losses and isolation of the two input ports of the six-port circuit in the frequency band of operation

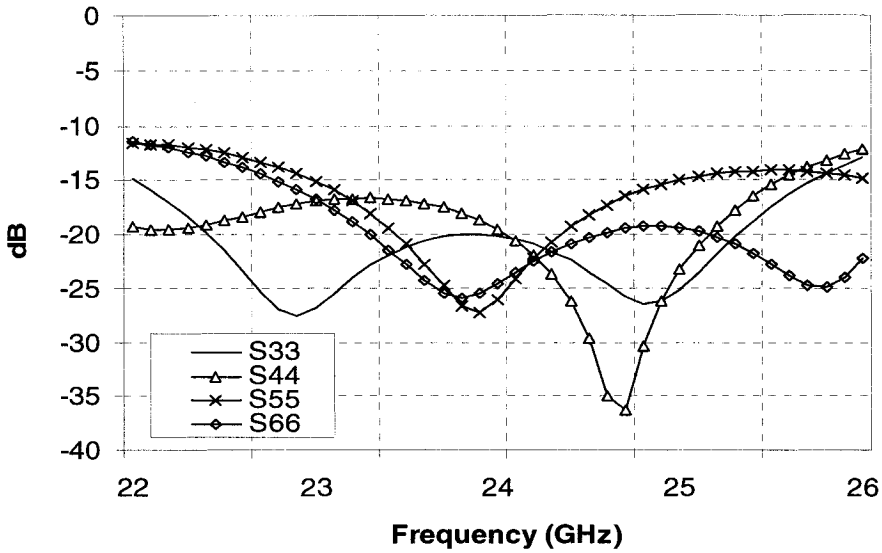


Figure 4.7 Simulated return losses of four output ports of the six-port circuit in the operating frequency band

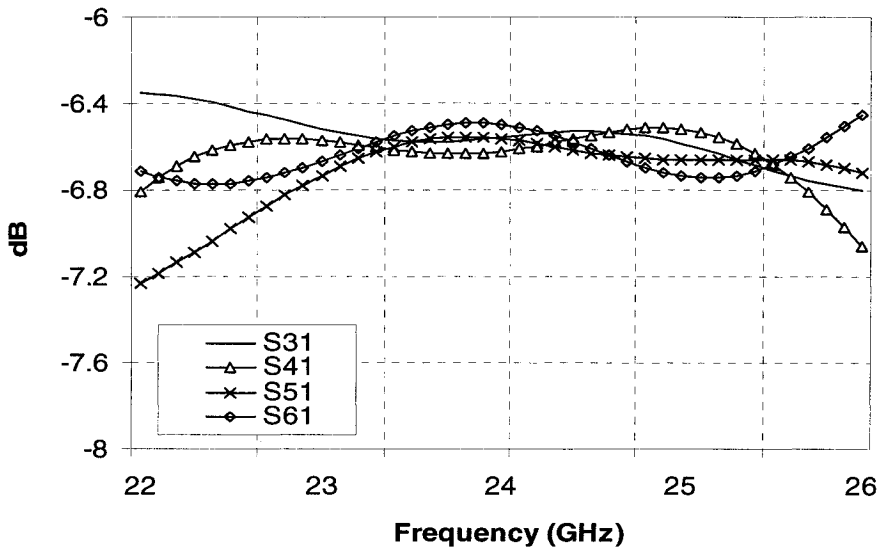


Figure 4.8 Simulated transmission parameters from port 1 to the output ports of the six-port circuit in the operating frequency band

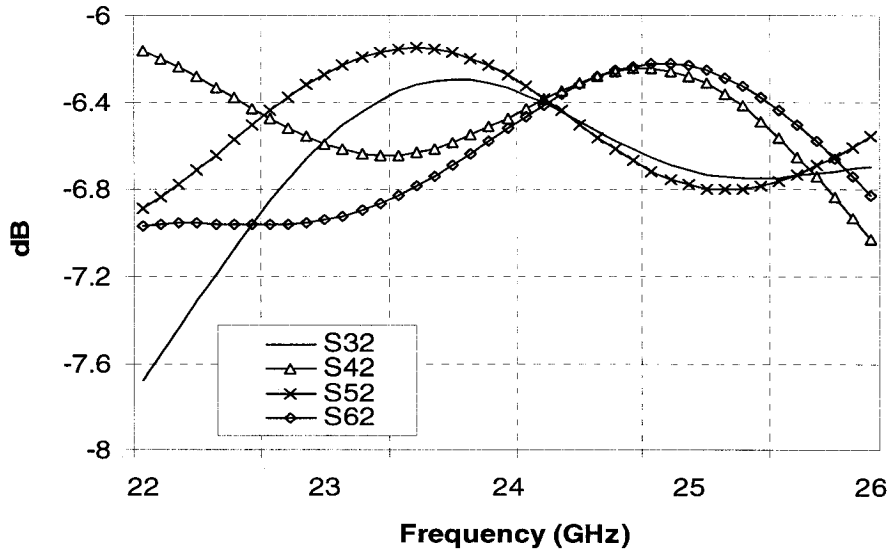


Figure 4.9 Simulated transmission parameters from port 2 to the output ports of the six-port circuit in the operating frequency band

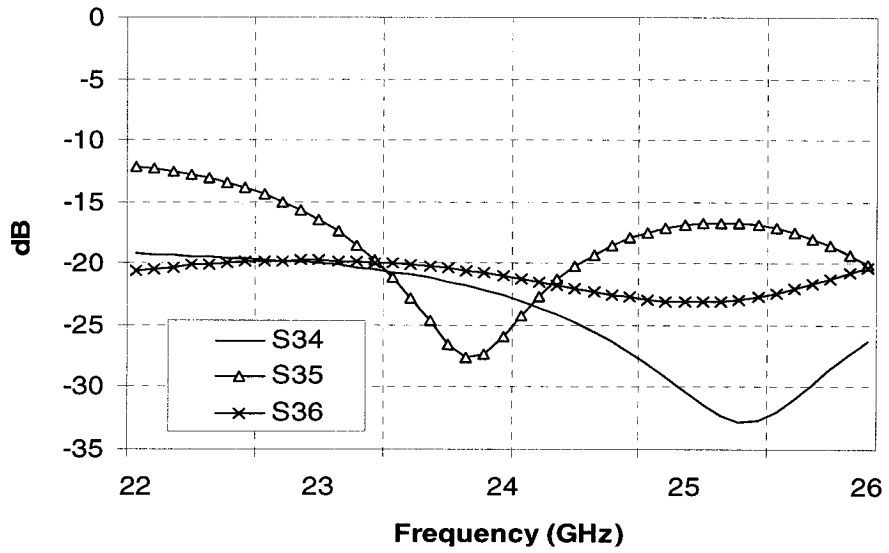


Figure 4.10 Simulated isolations between output ports of the six-port circuit in the operating frequency band

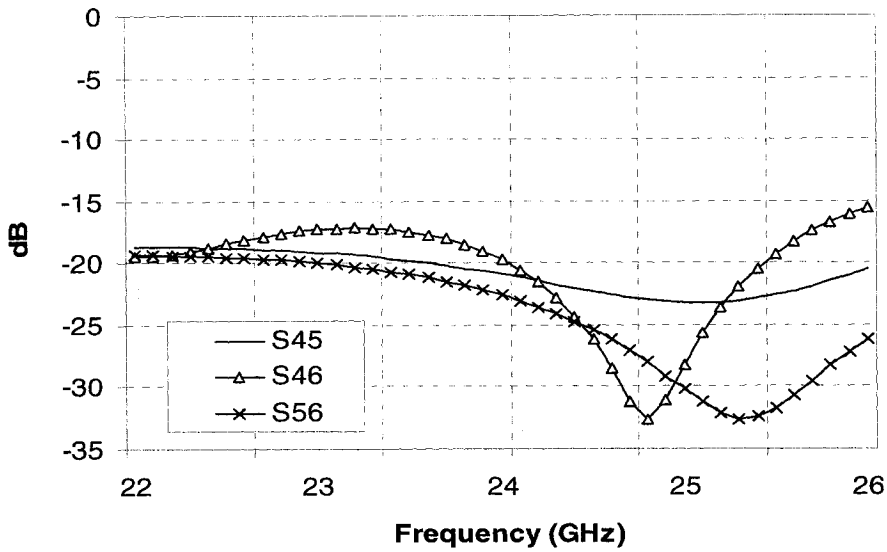


Figure 4.11 Simulated isolations between output ports of the six-port circuit in the operating frequency band

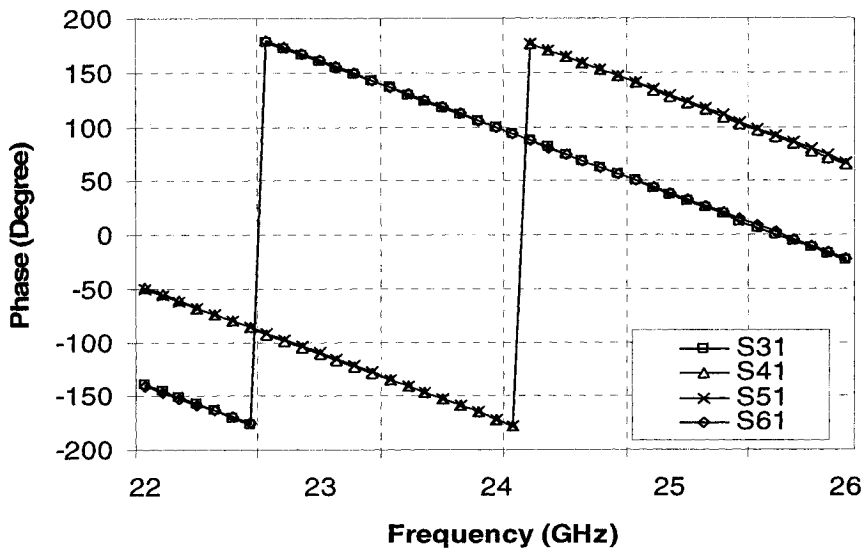


Figure 4.12 Simulated phase of transmission parameters from port 1 to the output ports of the six-port circuit in the operating frequency band

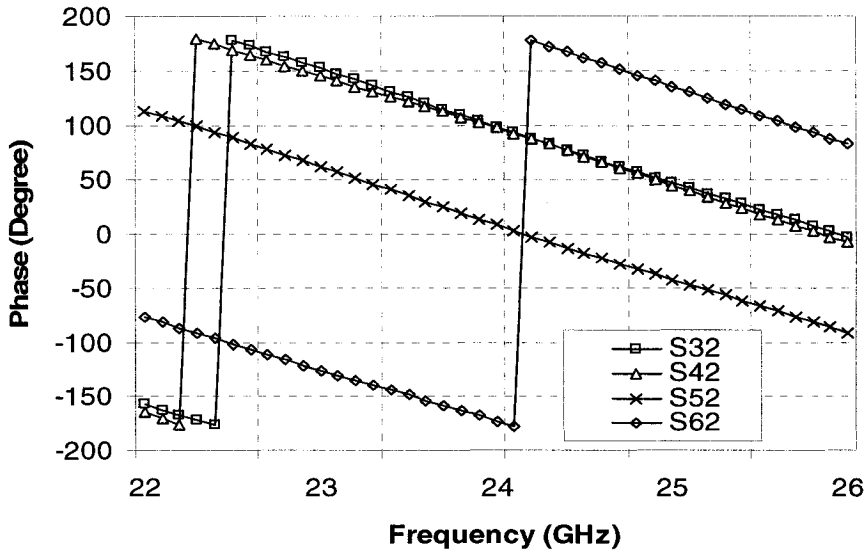


Figure 4.13 Simulated phases of transmission parameters from port 2 to the output ports of the six-port circuit in the operating frequency band

Figures 4.8 and 4.9 show the transmission parameters from port 1 and port 2 to the four output ports (S_{31}, S_{41}, S_{51}, S_{61}, S_{32}, S_{42}, S_{52}, S_{62}) in the operating frequency band. It can be seen that at the center frequency, the transmission parameters are around -6.5 dB which is very close to the theoretical values (-6 dB), and in the entire frequency band, the transmission parameters values stay in an acceptable range.

Figures 4.10 and 4.11 show isolations between output ports in the operating frequency band. It is found that the isolation between output ports is very good; the isolations value are lower than -20dB at the center frequency.

Figures 4.12 and 4.13 show the phases of the transmission parameters from ports 1 and 2 to four output ports in the operating frequency band, it can be found that the phase differences of the transmission parameters between the four output ports are excellent and match the theoretical values well in the entire frequency band.

4.5 Measurements of the microstrip six-port circuit

The designed six-port circuit is fabricated on ceramic substrate with relative permittivity $\varepsilon_r = 9.9$. The prototype of the microstrip six-port circuit for S-parameters measurement is shown in Figure 4.14. An Anrithsu test fixture and a HP-8510 network analyzer are used for S-parameters measurements.

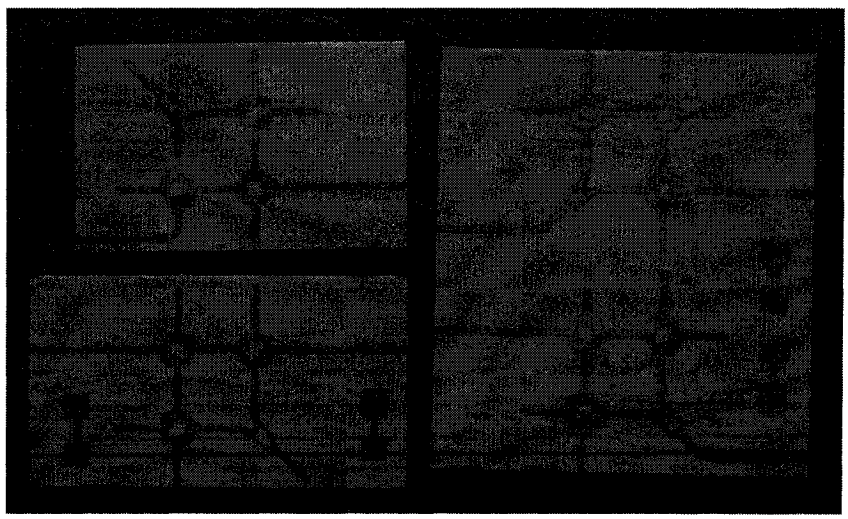


Figure 4.14 Prototype of the microstrip six-port circuit for S-parameters measurement

Simulated and measured S-parameters of the six-port circuit are summarized in Table 4.4, for a center frequency at 24 GHz. The reflection coefficients S_{11}, S_{22} are less than –26 dB and the isolation between RF port and LO port S_{12} is less than –28 dB. The transmission coefficients are close to the theoretically predicted value (-6 dB).

Table 4.4 Measured and simulated S-parameters of the MHMIC microstrip six-port

S-parameters	Simulated (dB)	Measured (dB)
S_{11}	-38.3	-27.5
S_{22}	-33.7	-26.8
S_{12}	-40.6	-28.8
S_{13}	-6.5	-6.4
S_{14}	-6.6	-6.4
S_{15}	-6.6	-6.5
S_{16}	-6.5	-6.3
S_{23}	-6.4	-6.5
S_{24}	-6.4	-6.4
S_{25}	-6.4	-6.6
S_{26}	-6.4	-6.3

Figure 4.15 shows measured return loss (S_{11}, S_{22}) and isolation (S_{12}) of the two input ports (port 1 and port 2) within the operating bandwidth. The return losses of port 1 and port 2 are lower than -25 dB, the isolation between the two input ports is -28 dB at center frequency and are lower than -15 db at most of the operating bandwidth.

Figure 4.16 shows the transmission parameters from port 1 and port 2 to the output ports (S_{61}, S_{52}) in the operating frequency band. It can be seen that at the center frequency, the transmission parameters are around -6.3 dB, which is very close to the theoretical value (-6 dB). In the entire frequency band, the differences of transmission parameter values to theoretical values are lower than 1dB.

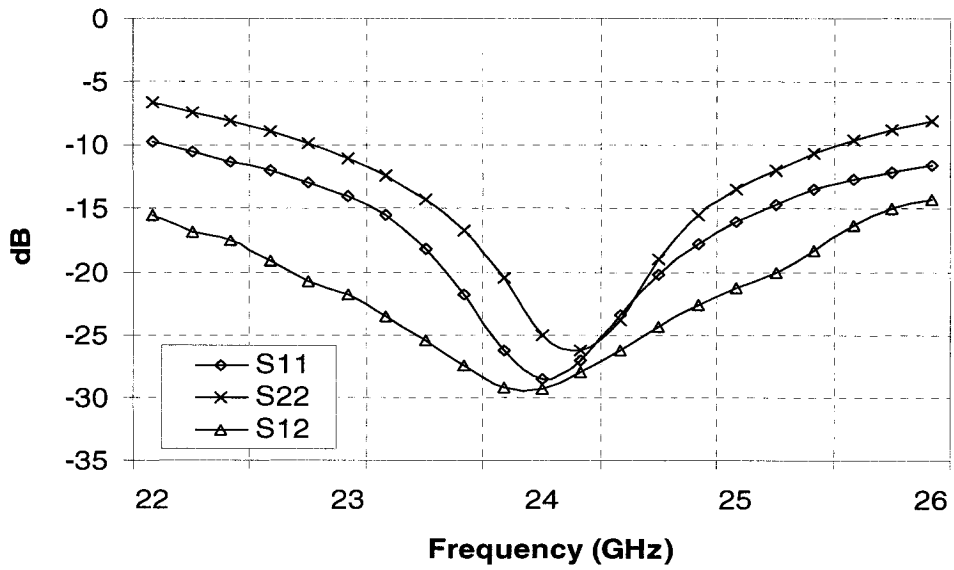


Figure 4.15 Measured return losses and isolation of the two input ports of the six-port circuit in the operating frequency band

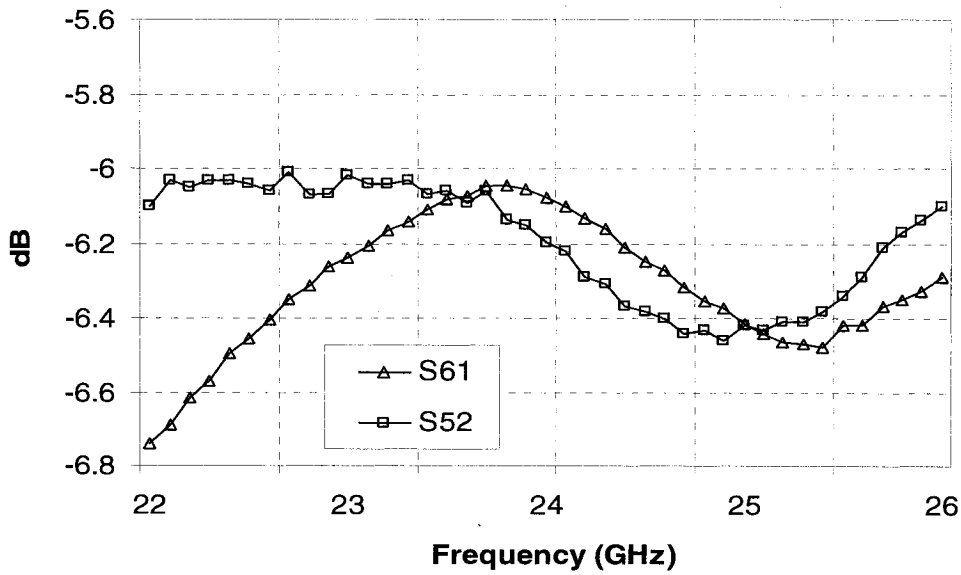


Figure 4.16 Measured transmission parameters from input ports to the output ports of the six-port circuit in the operating frequency band

CHAPTER V

SUBSTRATE INTEGRATED WAVEGUIDE SIX-PORT CIRCUIT DESIGN

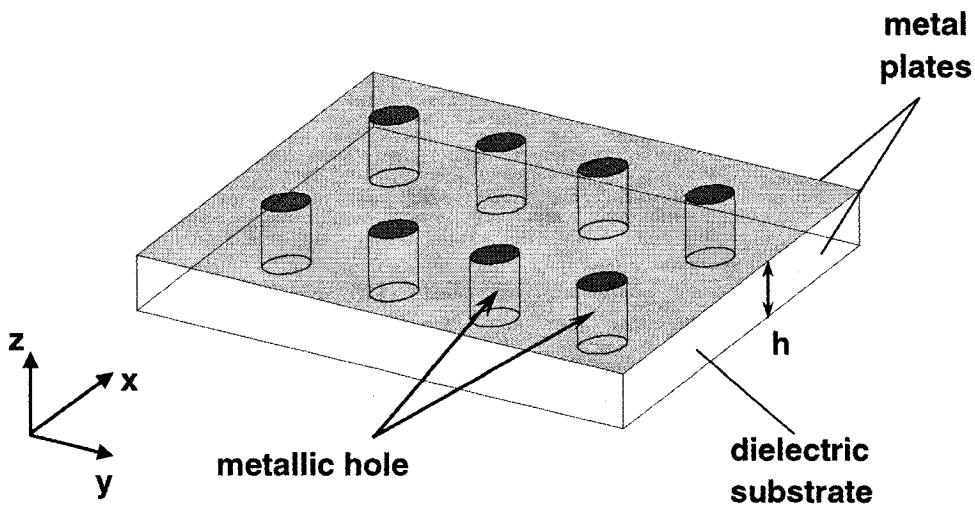
5.1 Introduction

Rectangular waveguide components have been widely used in millimeter wave systems, their relatively high cost and difficult integration prevent them from being used in low-cost high-volume applications. The substrate integrated waveguide (SIW) concept, which has been proposed [15], [31] recently as an attractive technology for low loss, low cost and high-density integration of microwave and millimeter wave components and sub-system, is appropriate for the design of six-port receiver and radar [9]. The SIW is a type of rectangular dielectric-filled waveguide that is synthesized in planar substrate with arrays of metallic vias to realize bilateral edge walls, and its transitions with planar structures [microstrip and coplanar waveguide (CPW), for example] are designed and integrated on the same substrate. In this case, the planar and non-planar structures can be integrated within the same planar platform, which leads to the design and development of low-cost millimeter wave integrated circuits (ICs) and systems [31]. In this way, a system can be integrated even in a package [i.e., system on package (SOP)], hence reducing size, weight, and cost, and greatly enhancing manufacturing repeatability and reliability.

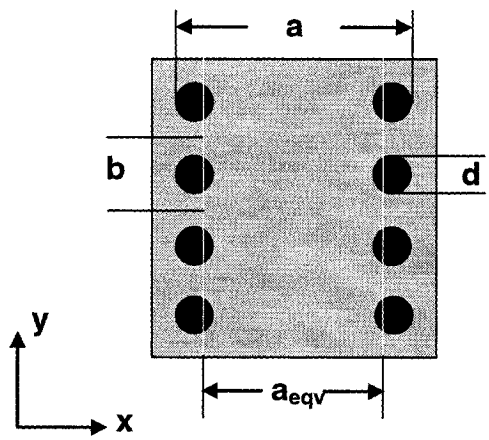
Although the periodic via structure of SIW is much more complicated for analysis compared with the conventional waveguide, it can be transformed to an equivalent rectangular waveguide with non-standard ratio of width/height [32]. By applying a generalized boundary integral-resonant mode expansion (BI-RME) method, the propagation characteristics of SIW can be obtained. It was demonstrated in [32] that a TE10-like mode in the SIW has dispersion characteristics that are almost identical with the TE10 mode of a dielectric filled rectangular waveguide with an equivalent width. This equivalent width, which is the effective width of the SIW, namely, a_{eqv} [see Figure 5.1(b)] can be approximated as follows:

$$a_{eqv} = a - d - \frac{d^2}{0.95 \cdot b} \tag{5.1}$$

Based on this property of SIW, existing design techniques for the rectangular waveguide can be used in a straightforward way to analyze and design various components knowing a_{eqv} of the SIW. This was proved in design of SIW cavities [33] and a series of SIW components that were designed using well-established rectangular waveguide design techniques.



(a)



(b)

Figure 5.1 Topology of SIW structure (a) solid view; (b) top view

A new SIW six-port circuit is presented in this chapter. It is designed based on the existing rectangular waveguide technique. Using the software High-Frequency Structure Simulator (HFSS) of Agilent Technologies, a six-port circuit is designed and simulated at the centre frequency of 24 GHz. The circuit is fabricated on a 0.508 mm thick

dielectric substrate with a relative permittivity ε_r = 2.2. An SIW power divider and an SIW coupler are designed as the fundamental building blocks for the proposed SIW six-port circuit. The six-port circuit prototype and geometrical parameters are given and simulated and measured results are presented.

As the fundamental building blocks of six-port circuit, the SIW power divider and the SIW hybrid 3 dB coupler are designed first.

5.2 SIW power divider

The topology of the SIW H-plane power divider is shown in Figure 5.2. A Y-junction straight structure [35] is adopted in the proposed SIW power divider. The power division section consists of a bifurcated waveguide junction fed by a symmetrical step junction. The SIW is converted to a conventional rectangular waveguide. The distance L between the two discontinuities and the input port width a_i can be optimized to achieve the power division and input specifications as required. A commercial finite element method (FEM) package is used for this optimization [36].

The power divider is optimized with two goals:

1) Minimize S_{11};

2) Keep S_{21} and S_{31} close to -3 dB.

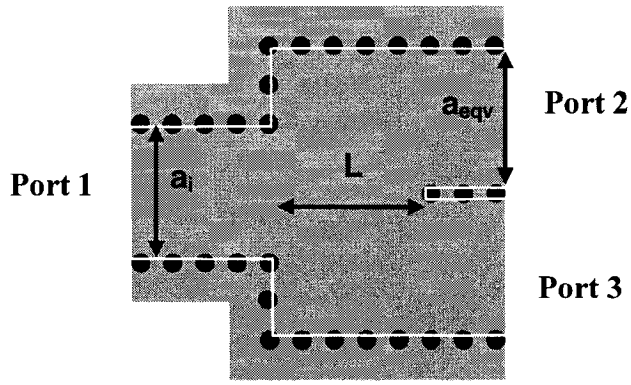


Figure 5.2 Topology of the SIW power divider

Three coefficients a_{eqv}, a_i and L are to be determined. First, the effective width of the output SIW, a_{eqv}, is calculated according to the substrate relative permittivity and the center frequency of the power divider; then the length L and the effective width of the input SIW a_i are optimized with respect to the minimum of S_{11}. Agilent Empipe3D Optimization software is used to optimize L and a_i to ensure that the S_{11} is lower than -20 dB over the whole bandwidth. Since the SIW power divider circuit is nearly lossless, S_{21} and S_{31} are close to -3dB. The final dimensions (see Figure 5.1 and Figure 5.2.) of the SIW power divider are listed in Table 5.1.

To test performance of the designed SIW power divider, the S-parameter simulation is made using HFSS at center frequency f_0 = 24 GHz. The simulated values are listed in Table 5.2.

Table 5.1 Physical dimensions of SIW power divider

a_i	5.449mm
b	1.5mm
h	0.508mm
d	0.8mm
L	6.744mm
a_{eqv}	5.8mm
ε_r	2.2

Table 5.2 Simulated S-parameters of SIW power divider

S-parameters	Magnitude	Phase
S11	0.0036 (-48.9 dB)	-159.3
S22	0.4987 (-6.04 dB)	-67.0
S33	0.4988 (-6.04 dB)	-67.1
S12=S21	0.7071 (-3.01 dB)	-89.9
S13=S31	0.7071 (-3.01 dB)	-89.9
S23=S32	0.501 (-6.00 dB)	113.2

It can be seen from the S-parameters that the proposed SIW power divider is matched to the input port (port 1) and the input signals are divided into two signals with equal amplitude and phase. As a lossless three-port system, two output ports (port 2 and port 3) of the SIW power divider are not matched, which will not affect the six-port circuit function as a direct receiver.

5.3 SIW hybrid coupler

The continuous aperture coupling design [37], [38] is applied in the design of SIW-based couplers. The coupling section consists of one continuous aperture and waveguide steps are used to achieve matching of the input ports. The SIW coupler topology is illustrated in Figure 5.3.

Similar to the design of the SIW power divider, the SIW is converted to a conventional rectangular waveguide. The aperture length (La), step width (Ws) and step length (Ls) are then optimized employing the FEM software [36] to achieve the coupling, isolation and input specifications as required. The two output ports of the coupler are sufficiently separated for machining two K connector holes.

The coupler is optimized with two goals:

1) Minimize S_{11} and S_{41} (at least -20 dB);

2) Keep S_{21} and S_{31} close to -3 dB.

The effective width of the output SIW, a_{eqv}, has already been determined for the power divider design and the three other parameters La, Ws and Ls are to be determined for the SIW coupler. First of all, the step width Ws is optimized to obtain an equal magnitude of S_{21} and S_{31}. Secondly, the aperture length La and step length Ls are optimized with

reference to the minimum of S_{41} and S_{11}. Since the value of Ls and La will also affect the power distribution of ports 2 and 3, it is necessary to repeat the first step and then the second step until those three parameters become convergent. Agilent Empipe3D Optimization software is again used to optimize Ws, La and Ls to ensure that S_{11} and S_{41} are lower than -20 dB and S_{21} and S_{31} are close to -3 dB in the whole frequency bandwidth. The final dimensions and parameters are obtained as listed in Table 5.3.

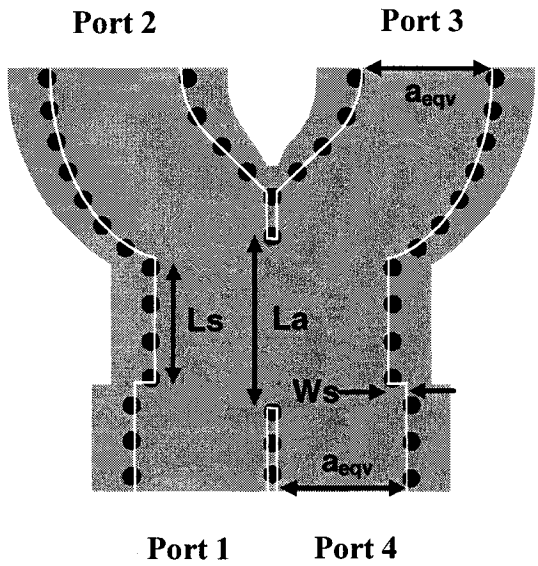


Figure 5.3 Topology of the SIW hybrid 3-dB coupler

S-parameters simulation of the designed SIW coupler is made using HFSS at center frequency f_0 = 24 GHz, and the comparison between simulated values and theoretic values are listed in Table 5.4.

Table 5.3 Physical dimensions of SIW hybrid coupler

a	5.467mm
b	1.5mm
h	0.508mm
d	0.8mm
La	7.411mm
Ls	5.376mm
Ws	0.869mm
a_{eqv}	5.8mm
ε_r	2.2

Table 5.4 Simulated and theoretic S-parameters of SIW hybrid coupler

S-parameters	Theoretic		Simulated	
	Magnitude	Phase (deg)	Magnitude	Phase (deg)
S_{11}	0	0	0.0044 (-47.1dB)	-131.3
S_{22}	0	0	0.0036 (-48.9dB)	-140.3
S_{33}	0	0	0.0050 (-46.0dB)	-138.6
S_{44}	0	0	0.0046 (-46.7dB)	-148.6
$S_{14} = S_{41}$	0	0	0.0043 (-47.3dB)	50.1
$S_{23} = S_{32}$	0	0	0.0045 (-46.9dB)	50.9
$S_{12} = S_{21}$	0,707 (-3dB)	-90	0.7083 (-3.00dB)	-89.5
$S_{13} = S_{31}$	0,707 (-3dB)	-180	0.7059 (-3.03dB)	-179.4
$S_{42} = S_{24}$	0,707 (-3dB)	-180	0.7059 (-3.03dB)	-179.5
$S_{43} = S_{34}$	0,707 (-3dB)	-90	0.7083 (-3.00dB)	-89.5

5.4 SIW to microstrip transition

As mentioned before, the advantage of the SIW circuit is its high-density integration, the entire circuit including planar circuit and waveguide can be constructed using standard printed circuit board (PCB) or other planar processing techniques. To realize this, a waveguide to microstrip transition with planar structures is designed. This transition structure uses a tapered microstrip line to excite the waveguide mode. The waveguide is synthesized on the dielectric substrate with linear arrays of metallized via holes. Since all the components are designed on the same dielectric substrate, a planar fabrication technique can guarantee excellent mechanical tolerances as well as tuning-free design.

Figure 5.4 shows the proposed transition from microstrip line to rectangular waveguide within a same dielectric substrate. The structure consists of a tapered microstrip line section that connects a 50 Ohm microstrip line and the integrated waveguide. The taper is used to transform the quasi-TEM mode of the microstrip line into the TE mode in the waveguide.

As indicated in Figure 5.5, the microstrip line is well suited to excite the waveguide because the electric fields of the two dissimilar structures are approximately oriented in the same direction and also they share the same profile. The design of such a transition is simple and straightforward. First, the size of the waveguide can be determined by considering the dielectric effect and well-established waveguide theory. The tapered

section is then designed to interrelate the line width of the 50 Ohm microstrip with the width of the integrated waveguide.

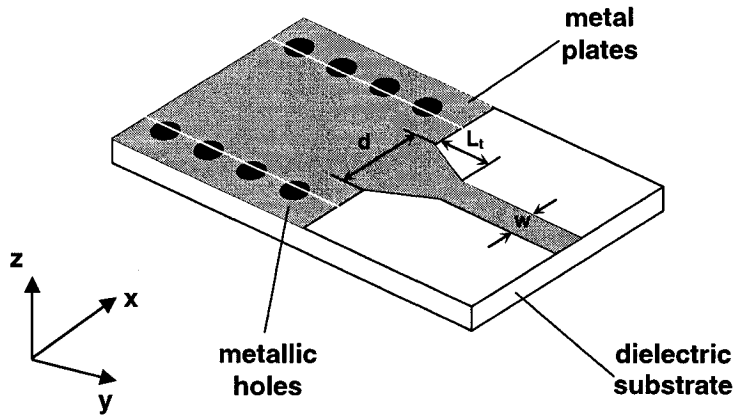


Figure 5.4 Transition from microstrip to rectangular waveguide within the same dielectric substrate

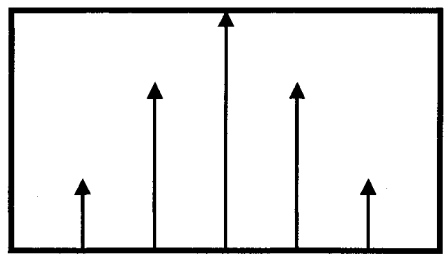


Figure 5.5 (a) Dominant modal electric field profile in the rectangular waveguide

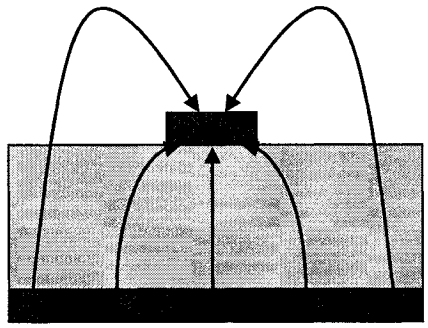


Figure 5.5 (b) Dominant modal electric field profiles in the microstrip line

S-parameter simulations of the designed SIW transition is made using HFSS at center frequency f_0 = 24 GHz. The simulated values are listed in Table 5.5.

Table 5.5 Simulated S-parameters of SIW transition

S-parameters	Magnitude	Phase
S11	0.0016 (-55.9 dB)	-81.0
S21	1.0000 (0 dB)	-36.9

To test performance of the designed SIW transition, a circuit which involves two proposed transitions and a 12 mm synthesized rectangular waveguide (topology is shown in Figure 5.6) was designed and its S-parameters simulation is made using HFSS. Figures 5.7 and 5.8 show the simulated results. A bandwidth of more than 40% of center frequency is obtained for 20 dB return loss from 20 to 30 GHz.

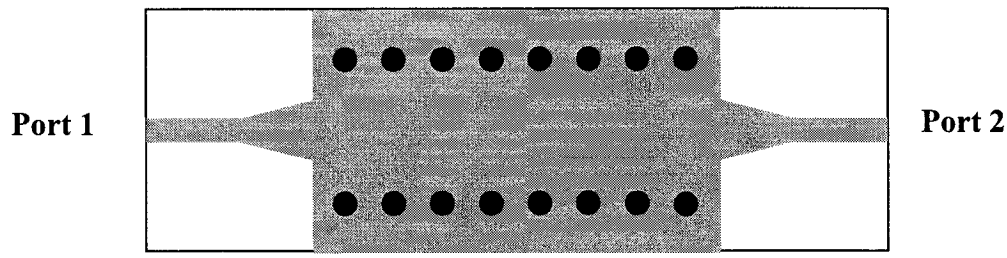


Figure 5.6 Two SIW transitions with a synthesized rectangular waveguide

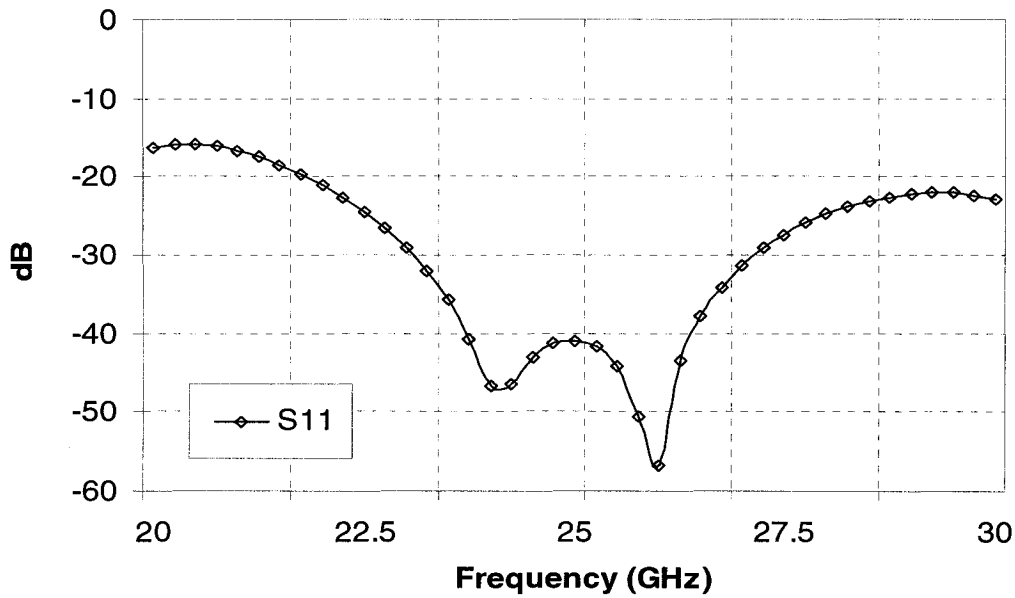


Figure 5.7 Simulated return loss (S_{11}) of SIW transition

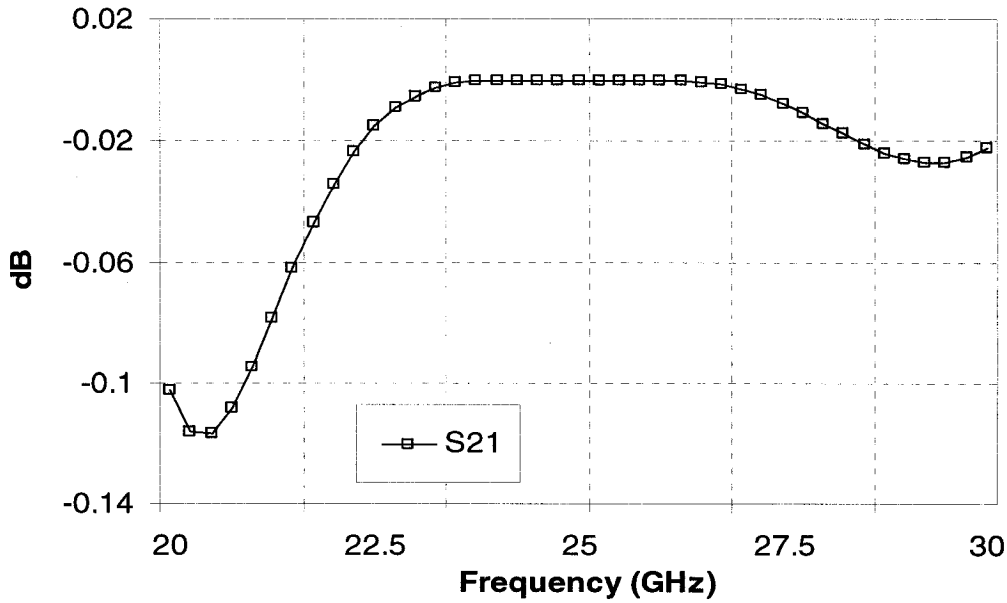


Figure 5.8 Simulated insertion loss (S21) of SIW transition

5.5 Simulated S-parameters of the six-port circuit

Adopting the six-port circuit model shown in Figure 3.3 (b), the presented SIW six-port circuit consists of two power dividers, two 90-degree 3-dB hybrid couplers and some phase shifters. The topology and block diagram of the proposed six-port circuit is shown in Figure 5.9. Additional SIW transmission lines are introduced to realize a 45 degree phase shift at the center frequency of 24 GHz. Microstrip-to-SIW transitions [39] are placed at each port of the circuit for measurement purpose.

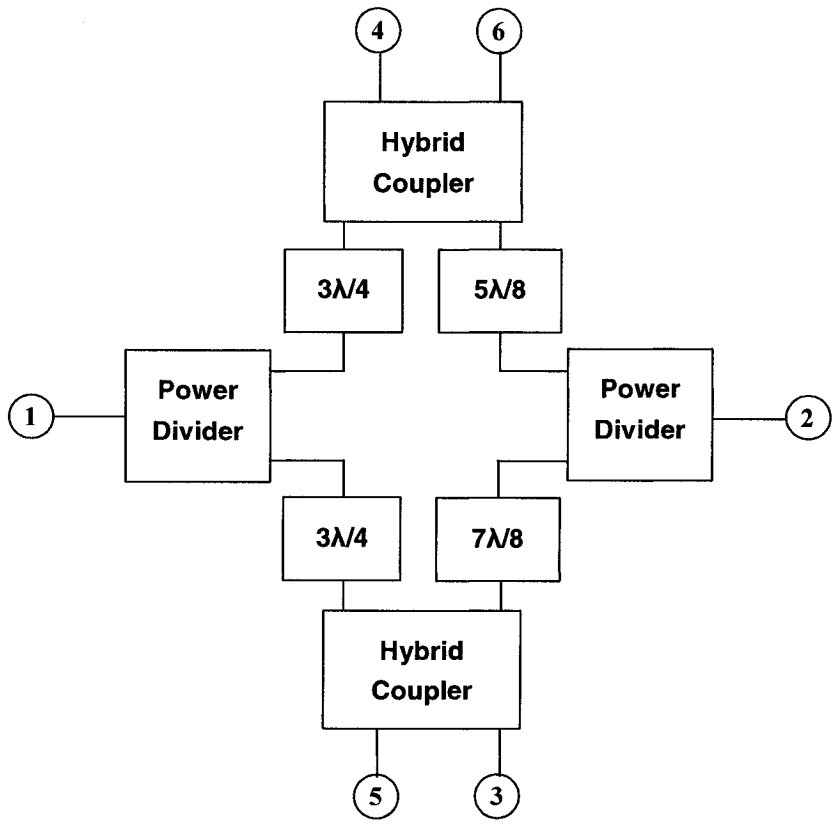


Figure 5.9 (a) Block diagram of SIW six-port circuit

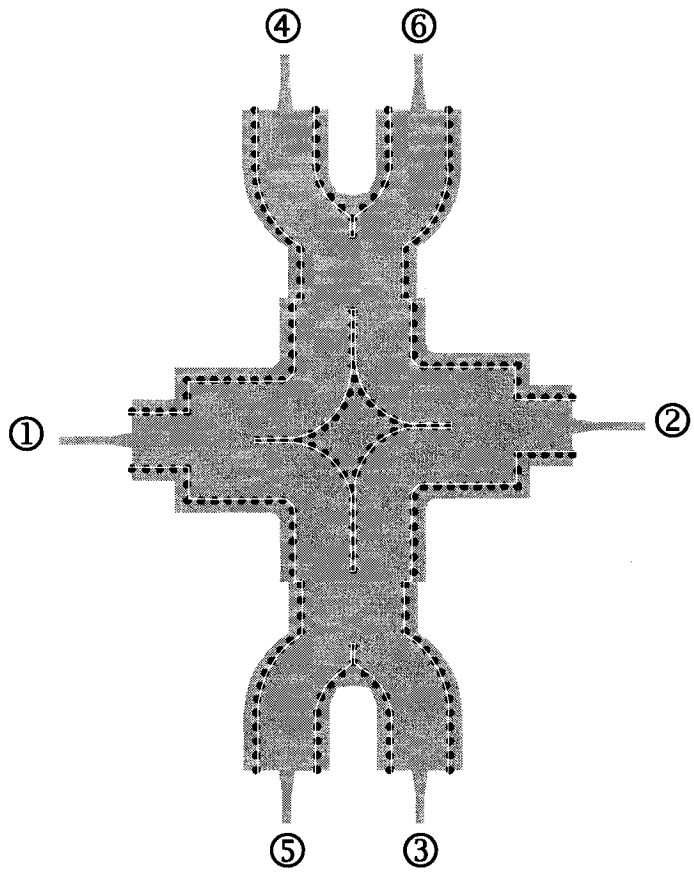


Figure 5.9 (b) The topology of SIW six-port circuit (with transitions)

Unlike other six-port circuits [11], [13] for direct receiver system, the proposed six-port structure is a real "six-port", without need for any external connected terminals. Therefore, the structure is more compact at lower cost.

The six-port circuit is designed with four goals:

1. Minimize S_{11} and S_{22}. The return losses of the designed six-port circuit should be lower than -20dB at the center frequency (24 GHz);

2. Minimize S_{12}, S_{53} and S_{46}. The isolation of ports 1 and 2, ports 5 and 3, as well as ports 4 and 6 should be lower than -20 dB at the center frequency of 24 GHz;
3. Keep the amplitude of S_{31} to S_{61} and S_{32} to S_{62} close to -6 dB for well-balanced outputs;
4. Keep the phase shift between the two input ports (port 1 and port 2) with respect to the four output ports (ports 3, 4, 5, 6) close to the theoretical values (see Table 5.6).

S-parameters simulation of the proposed six-port circuit was made using HFSS at center frequency f_0 = 24 GHz, and the comparison between simulated values and theoretic values are listed in Table 5.6.

From Table 5.6, we discover that the proposed six-port circuit matches very well at the input ports (S_{11}, S_{22} are less than -30 dB), and the isolation of the two input ports is excellent (S_{12} is less than -39 dB). At the same time, the transfer parameters (S_{31}, S_{41}, S_{51}, S_{61}, S_{32}, S_{42}, S_{52}, S_{62}) are very close to the theoretical values. As mentioned before, the two output ports of the SIW power divider are not matched, making the four output ports (ports 3, 4, 5, 6) of the SIW six-port circuit not matched. Since these four output ports will connect to power detectors, and there is no signal input to these four ports, this mismatch will not affect the six-port circuit's functionality as a direct receiver.

Same as the MHMIC six-port circuit, the SIW six-port circuit is designed at center frequency 24 GHz and with 4 GHz (22-26 GHz) bandwidth.

Table 5.6 Simulated S-parameters of SIW six-port circuit

S-parameters	Theoretic		Simulated	
	Magnitude	Phase (deg)	Magnitude	Phase (deg)
S11	0	0	0.0073 (-42.7dB)	-130.8
S22	0	0	0.0304 (-30.3dB)	-101.3
S12	0	0	0.011 (-39.2dB)	172.4
S31	0.5 (-6 dB)	-180	0.4964 (-6.1dB)	-179.3
S41	0.5 (-6 dB)	-90	0.5029 (-6.0dB)	-89.0
S51	0.5 (-6 dB)	-90	0.504 (-6.0dB)	-90.0
S61	0.5 (-6 dB)	-180	0.4963 (-6.1dB)	-180.4
S32	0.5 (-6 dB)	-135	0.4951 (-6.1dB)	-134.8
S42	0.5 (-6 dB)	-135	0.5049 (-5.9dB)	-134.9
S52	0.5 (-6 dB)	135	0.4998 (-6.0dB)	135.4
S62	0.5 (-6 dB)	-45	0.4991 (-6.0dB)	-44.2

The SIW six-port circuit is simulated using HFSS 5.6, the simulation model includes SIW power dividers, SIW couplers, SIW phase shifters and SIW-to-Microstrip transitions. All the SIW components are modeled using the equivalent rectangular waveguide with effective width a_{eqv}. Considering the time-efficiency of simulation, the K connectors are not included in the HFSS simulation model, while the measured results naturally involve effects of the K connectors at each port. The simulated S-parameters of the SIW six-port circuit are shown in Figure 5.10 ~ Figure 5.14.

Figure 5.10 shows the return loss (S_{11}, S_{22}) and the isolation (S_{12}) of the two input ports (port 1 and port 2) within the operating bandwidth. It can be found from the figure that the return losses of port 1 and port 2 are lower than -27 dB at the center frequency (24 GHz) and are lower than -15 dB in all the operating frequency bandwidth. The isolation between the two input ports is -35 dB at center frequency and is lower than -17 dB at almost all the frequency band.

Figures 5.11 and 5.12 show transmission parameters from port 1 and port 2 to the four output ports (S_{31}, S_{41}, S_{51}, S_{61}, S_{32}, S_{42}, S_{52}, S_{62}) in the operating frequency band. It can be seen that at center frequency, the transmission parameters are around -6.0 dB, which is very close to the theoretical values, and in the entire frequency band, the transmission parameters values stay within an acceptable range.

Figures 5.13 and 5.14 show the phase of the transmission parameters from ports 1 and 2 to four output ports in the operating frequency band. We can find that the transmission parameters phase differences between the four output ports are excellent and match well with the theoretical values in the entire frequency band.

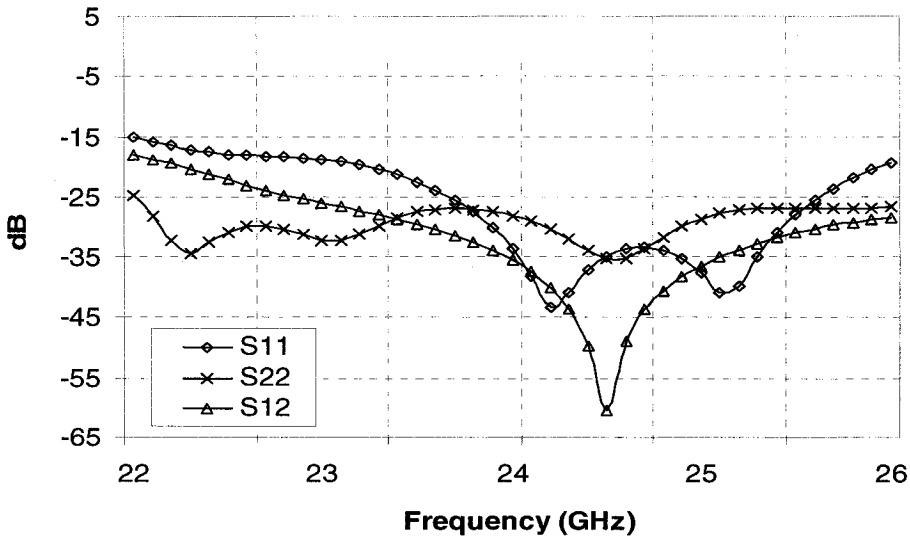


Figure 5.10 Simulated return losses and isolation of the two input ports of the six-port circuit in the operating frequency band

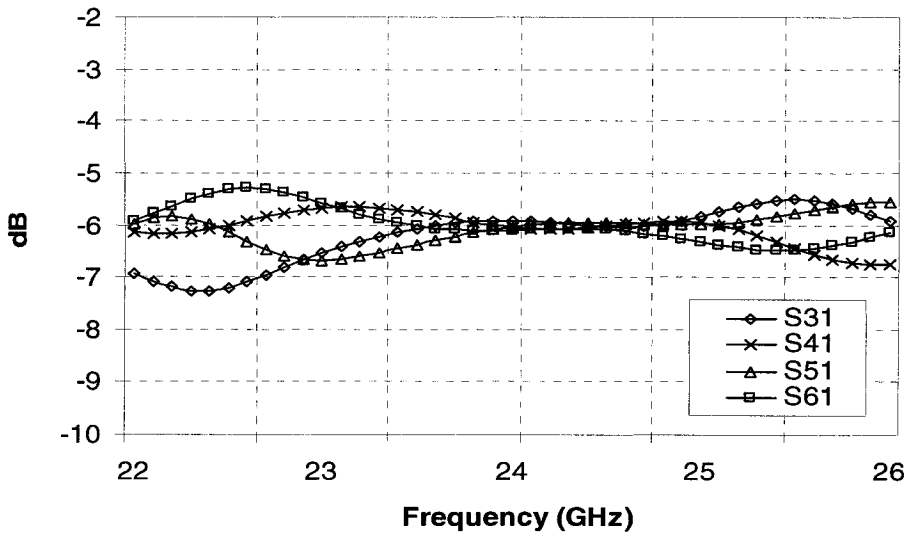


Figure 5.11 Simulated transmission parameters from port 1 to the output ports of the SIW six-port circuit in the operating frequency band

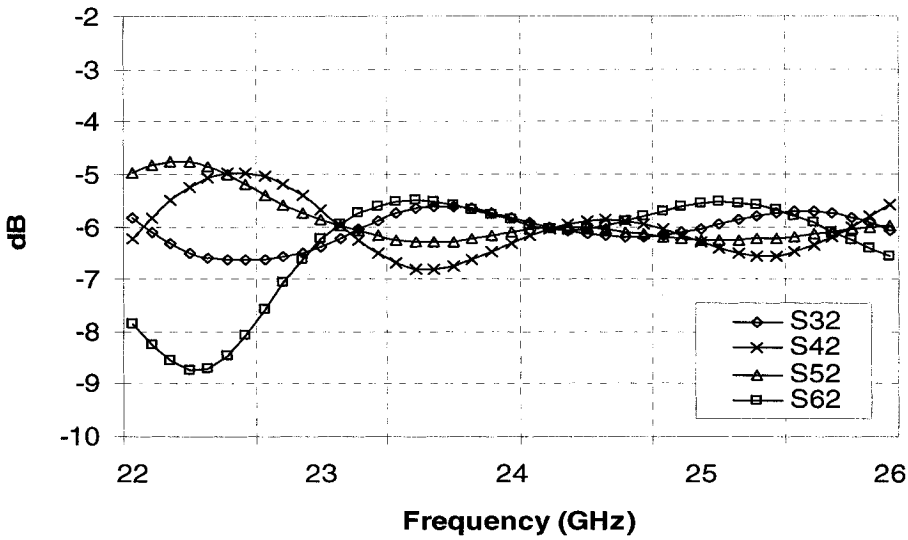


Figure 5.12 Simulated transmission parameters from port 2 to the output ports of the SIW six-port circuit in the operating frequency band

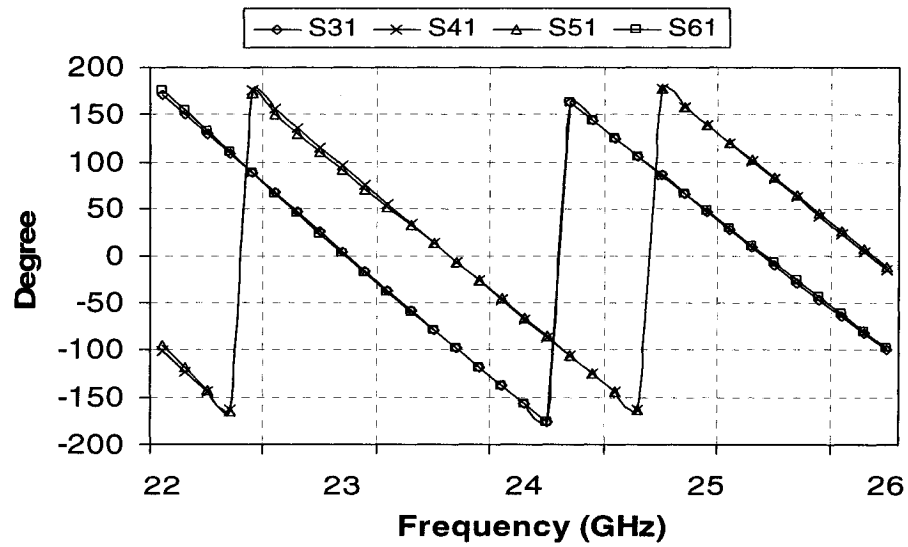


Figure 5.13 Simulated phases of transmission parameters from port 1 to the output ports of the SIW six-port circuit in the operating frequency band

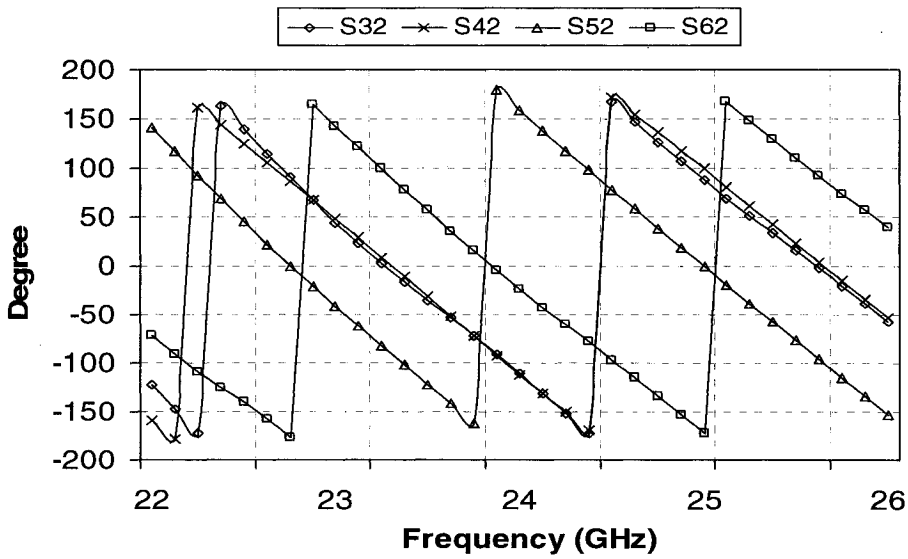


Figure 5.14 Simulated phases of transmission parameters from port 2 to the output ports of the SIW six-port circuit in the operating frequency band

5.6 Measurements of the SIW six-port circuit

An actual SIW six-port circuit is fabricated and measured on a Rogers RT/duroid 5880 Laminates substrate with a relative permittivity $\varepsilon_r = 2.2$. The prototype of the SIW six-port circuit is illustrated in Figure 5.15.

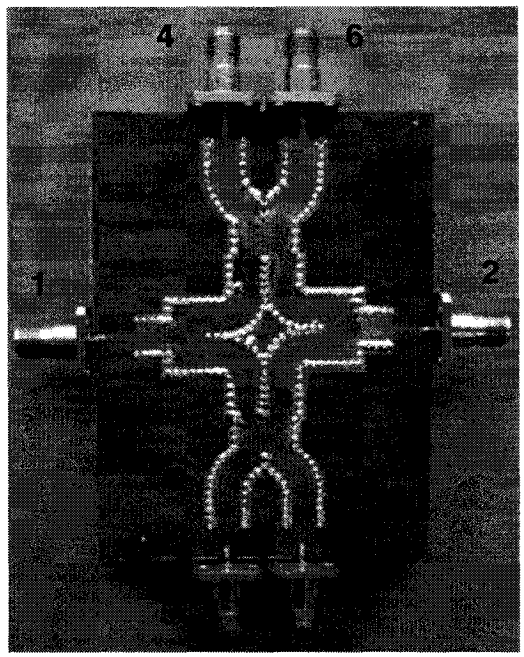


Figure 5.15 Prototype of the SIW six-port circuit (with connectors)

An HP8150 network analyzer is used for S-parameters measurements. K connectors are placed at each port of the circuit for measurement purpose. Port 1 and port 2 are connected to the received RF signals and LO, respectively. The other four ports (ports 3~6) are output ports and are connected to power detectors. The output power levels of these four ports will be used to determine the RF signals. Simulated and measured S-parameters of the six-port circuit are summarized in Table 5.7, and the measured S-parameters of the SIW six-port circuit over the operating frequency band are shown in Figure 5.16 ~ Figure 5.20.

It can be found from Table 5.7 that at the center frequency, the reflection coefficients S_{11}, S_{22} are less than –21 dB and the isolation between the RF port and the LO port S_{12} is less than –21 dB. The transmission coefficients are close to the theoretically predicted value

Table 5.7 Measured and simulated S-parameters of SIW six-port

S-parameters	Simulated (dB)	Measured (dB)
S11	-42.7	-25.3
S22	-30.7	-21.0
S12	-39.2	-21.2
S13	-6.1	-6.6
S14	-6.0	-6.5
S15	-6.0	-8.0
S16	-6.1	-8.6
S23	-6.1	-8.3
S24	-5.9	-7.7
S25	-6.0	-7.3
S26	-6.0	-6.3

Figure 5.16 shows measured S_{11} and S_{22} (which represent return loss) and S_{21} (which represents isolation between two RF ports) of the proposed SIW six-port circuit. It can be seen that at center frequency, the return loss of these two ports is lower than -20 dB and the isolation is lower than -26 dB. Figure 5.17 presents measured S_{31} to S_{61} (represent the transmission coefficients of port 1 to the output ports) of the proposed SIW six-port circuit. The transmission coefficients are found close to the theoretically predicted value (-6 dB) over the operating frequency band.

Figure 5.18 gives measured S_{32} to S_{62} (represent the transmission coefficients of port 2 the to the output ports) of the proposed six-port circuit. Same as the transmission coefficients of port 1 to the output ports, the transmission coefficients of port 2 to the output ports are close to the theoretically predicted value (-6 dB) over the operating frequency band.

Figures 5.19 and 5.20 show measured phase of transmission parameters from port 1, 2 to the four output ports in the operating frequency band. We can find that the transmission parameters phase differences between four output ports are well matched with theoretical values over the entire frequency band.

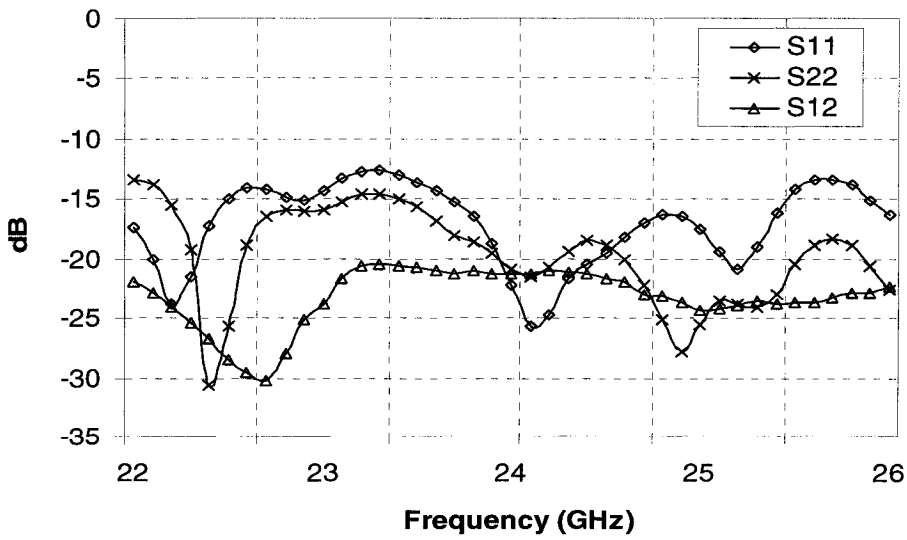


Figure 5.16 Measured return losses and isolation of the two input ports of the six-port circuit in the operating frequency band

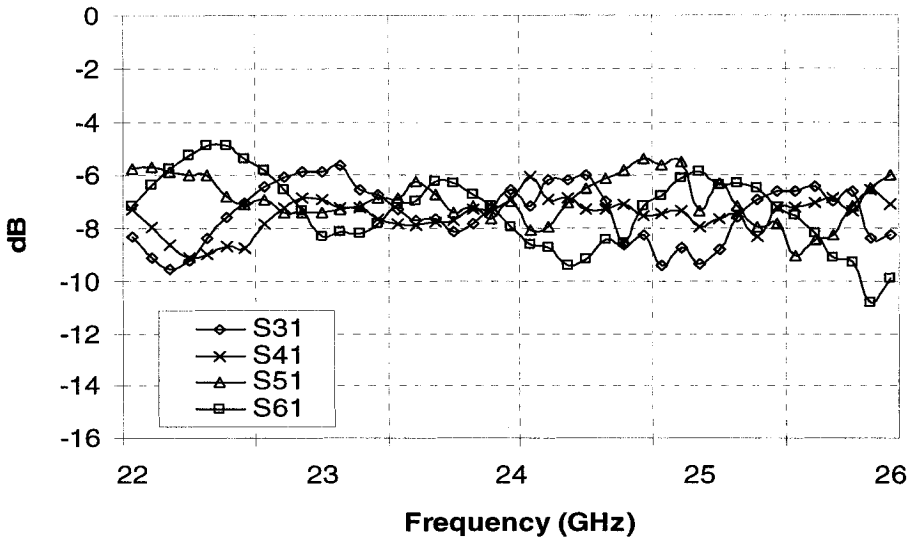


Figure 5.17 Measured transmission parameters from port 1 to the output ports of the SIW six-port circuit in the operating frequency band

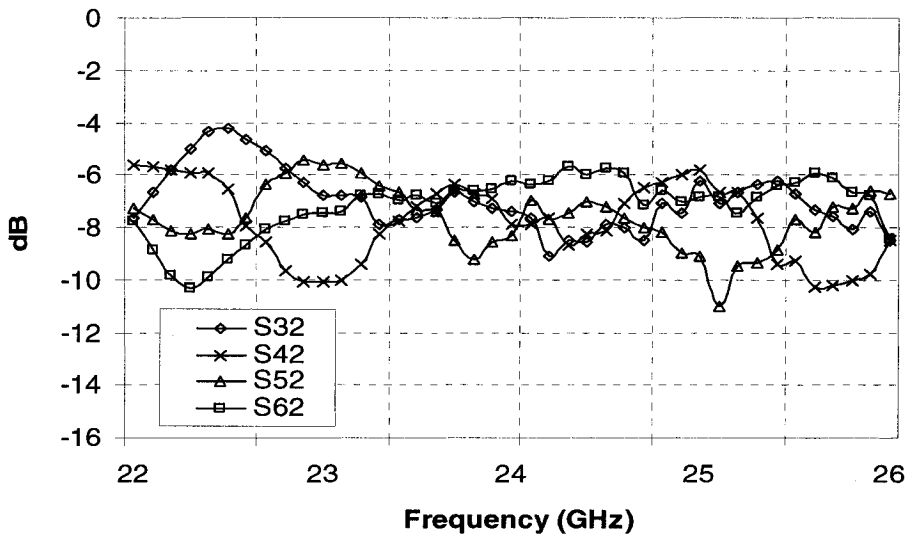


Figure 5.18 Measured transmission parameters from port 2 to the output ports of the SIW six-port circuit in the operating frequency band

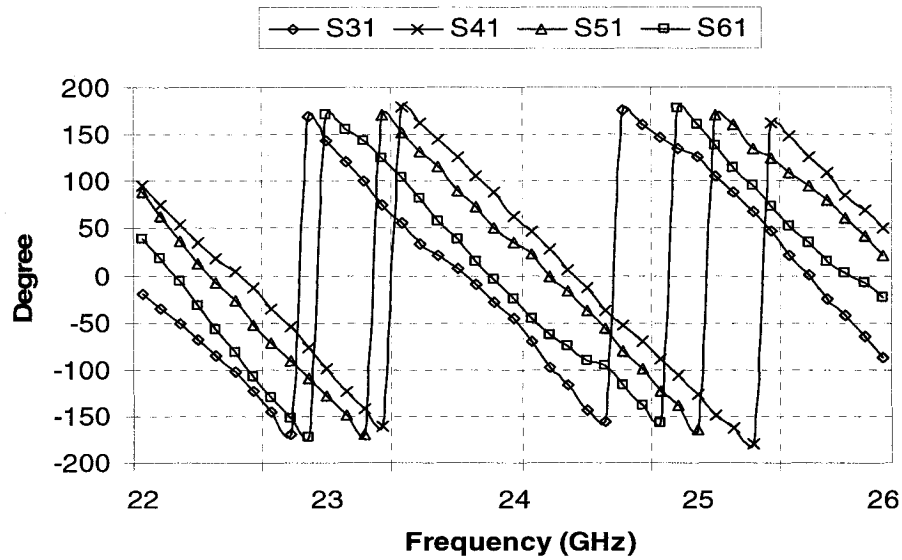


Figure 5.19 Measured phase of transmission parameters from port 1 to the output ports of the SIW six-port circuit in the operating frequency band

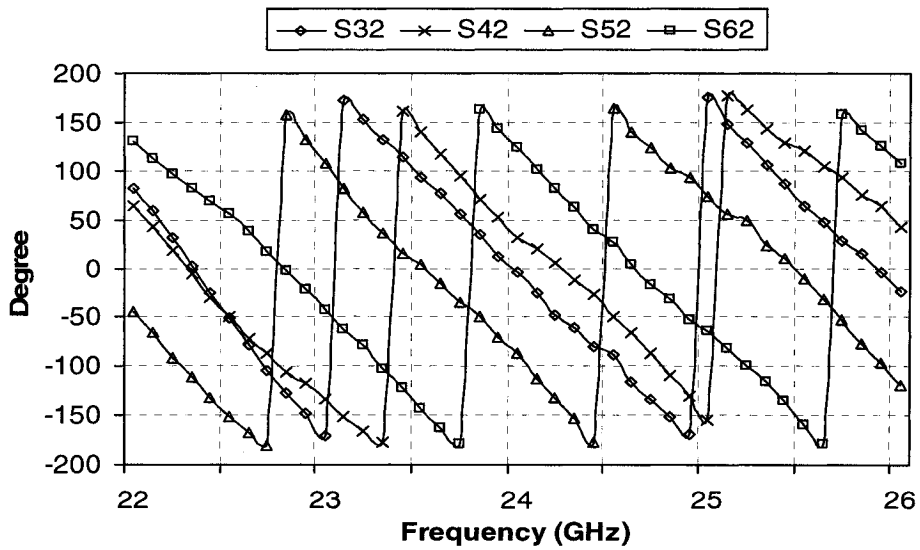


Figure 5.20 Measured phase of transmission parameters from port 2 to the output ports of the SIW six-port circuit in the operating frequency band

5.7 Comparison of microstrip six-port and SIW six-port

An SIW six-port is proposed for the first time for SDR receiver platform. It gives a novel method of six-port design at millimeter wave frequency. Comparing with a microstrip structure, the SIW structure can achieve higher Q value which means smaller energy loss of the whole circuit. Simulated results show that the SIW structure can achieve smaller insertion loss between the RF input port and the power detector ports, and more isolation between the RF input port and the LO port. In addition, the SIW structure can work at higher frequency over 30 GHz, while the high loss of microstrip circuit makes it unacceptable at frequency lever that over 30 GHz.

As an SIW structure, it can effectively be converted to an equivalent conventional rectangular waveguide. The SIW can then be modeled by conventional waveguide techniques and all the existing design methods for the rectangular waveguide can be applied. With an appropriate choice of via pith and diameter, the radiation loss can be decreased to a negligible level. All these characteristics make the SIW structure a good solution for an SDR working at a high frequency band, especially at the millimeter wave band.

On the other hand, the size of SIW six-port circuit is much larger compared to a microstrip six-port circuit. As we know, the size of the six-port circuit is related to the

working frequency, which means that the SIW structure is not adopted to low frequency communication, and a microstrip structure six-port may be a better choice in such a situation.

CHAPTER VI

SDR RECEIVER ALGORITHMS

6.1 Introduction

As shown in equation (3.15), the ratio of amplitude, frequency and phase between the LO signal (port 1) and the RF signal (port 2) can be calculated from the output power levels at the other four ports with the complex constants X_i, Y_i known by calibration procedures. In the past, many algorithms have been proposed for offline and online calibration of six-port circuit. In this chapter, six-port computation algorithms, six-port calibration methods and receiver demodulation results for different modulation schemes will be presented and discussed.

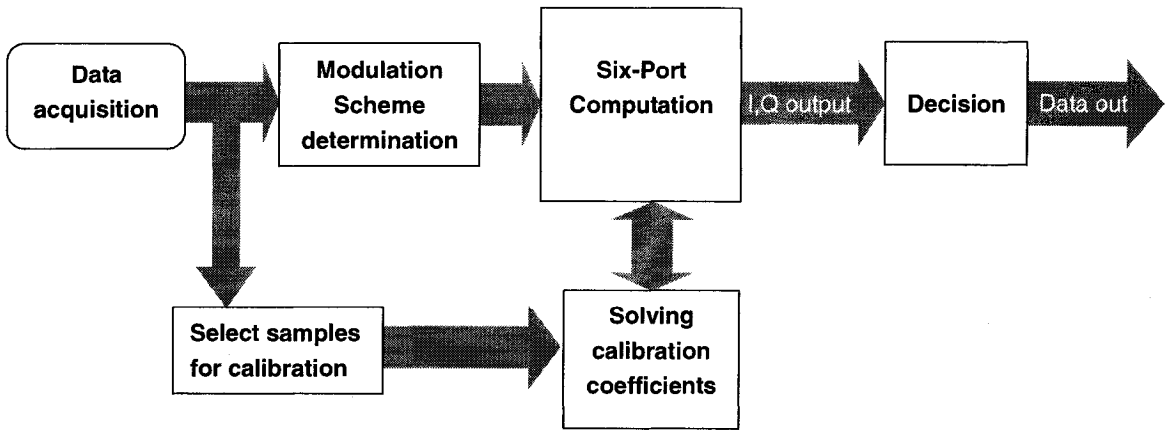


Figure 6.1 Flow chart of six-port receiver algorithm

Figure 6.1 shows the algorithm flow chart of an SDR six-port receiver. After the data is acquired from the antenna, some samples are selected for calibration. From calibration, the six-port calibration coefficients can be generated. The coefficients are then applied in six-port computation to calculate the I-Q data. Following a decision algorithm, the signals are then demodulated. This process is an universal demodulation algorithm for six-port receivers. However, in certain cases, for instance for some modulation schemes, the calibration coefficients are not necessary for six-port computation. In this way, the calibration procedure can be omitted and the demodulation algorithm could be simplified. In following part of this chapter, some calibration methods are presented and then demodulation results for the six-port receiver are given, some simplified demodulation algorithms for certain modulation schemes are presented and discussed at the end of the chapter.

6.2 Six-port computation

For a six-port receiver, port 1 and port 2 are connected to the LO and the RF signal. For an I-Q amplitude modulation scheme, we can define the time domain RF and LO signals as follows:

$$V_{RF}(t) = \mathrm{Re}\left(A_{RF}\left(I(t) + jQ(t)\right)e^{j\Phi_{RF}(t)}\right) \tag{6.1}$$

$$\Phi_{RF}(t) = w_{RF}t + \varphi_{RF} \tag{6.2}$$

$$V_{LO}(t) = \mathrm{Re}\left(A_{LO} e^{j\Phi_{LO}(t)} \right) \tag{6.3}$$

$$\Phi_{LO}(t) = w_{LO} t + \varphi_{LO} \tag{6.4}$$

Consider the SIW six-port circuit proposed in Chapter 5 (see Figure 6.2). The theoretical S-parameters from port 1 and port 2 to the four output ports are shown in Table 6.1.

Table 6.1 S-parameters from port 1 and port 2 to the four output ports

Ports	3	4	5	6
1 (LO)	0.5 / -180	0.5 / -90	0.5 / -90	0.5 / -180
2 (RF)	0.5 / -135	0.5 / -135	0.5 / 135	0.5 / -45

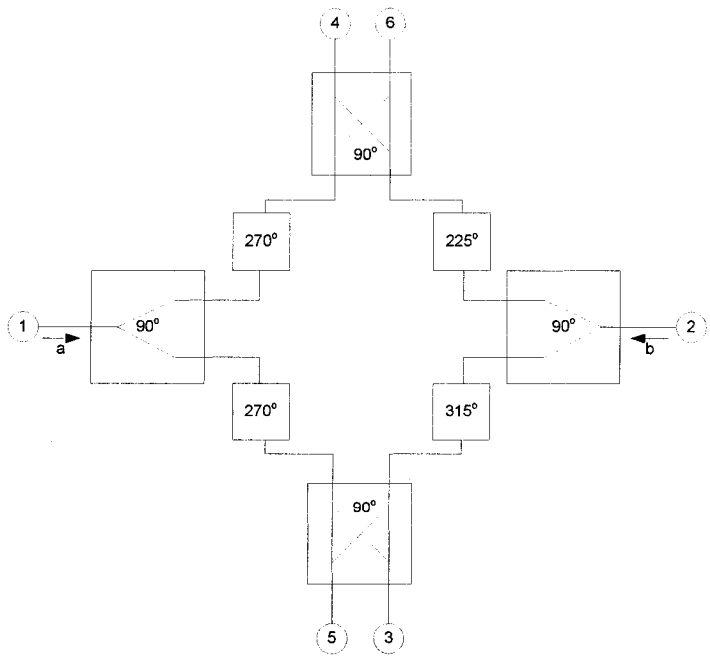


Figure 6.2 Block diagram of the proposed SIW six-port circuit

Consider that the six-port receiver is ideal and there is no loss and no noise (block diagram shown in Figure 6.3). From Table 6.1, when the LO and RF signals are connected to port 1 and port 2, the signal voltages of the four output ports (ports 3 - 6) are described in equation (6.5) – (6.8).

$$V_3(t) = \mathrm{Re}\left(\frac{A_{RF}}{2} e^{j(\Phi_{RF}(t)-\frac{3\pi}{4})} \left(I(t)+jQ(t)\right) + \frac{A_{LO}}{2} e^{j(\Phi_{LO}(t)-\pi)} \right) \tag{6.5}$$

$$V_4(t) = \mathrm{Re}\left(\frac{A_{RF}}{2} e^{j(\Phi_{RF}(t)-\frac{3\pi}{4})} \left(I(t)+jQ(t)\right) + \frac{A_{LO}}{2} e^{j(\Phi_{LO}(t)-\frac{\pi}{2})} \right) \tag{6.6}$$

$$V_5(t) = \mathrm{Re}\left(\frac{A_{RF}}{2} e^{j(\Phi_{RF}(t)+\frac{3\pi}{4})} \left(I(t)+jQ(t)\right) + \frac{A_{LO}}{2} e^{j(\Phi_{LO}(t)-\frac{\pi}{2})} \right) \tag{6.7}$$

$$V_6(t) = \mathrm{Re}\left(\frac{A_{RF}}{2} e^{j(\Phi_{RF}(t)-\frac{\pi}{4})} \left(I(t)+jQ(t)\right) + \frac{A_{LO}}{2} e^{j(\Phi_{LO}(t)-\pi)} \right) \tag{6.8}$$

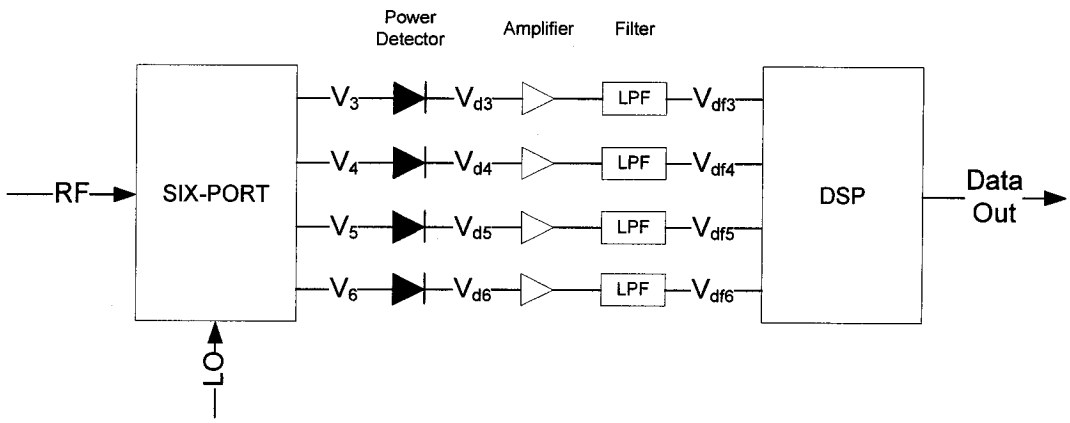


Figure 6.3 Six-port receiver

By expanding equation (6.5) – (6.8), we get:

$$V_3(t)=\frac{A_{RF}}{2}\cos\left(\Phi_{RF}(t)-\frac{3\pi}{4}\right)I(t)-\frac{A_{RF}}{2}\sin\left(\Phi_{RF}(t)-\frac{3\pi}{4}\right)Q(t)+\frac{A_{LO}}{2}\cos\left(\Phi_{LO}(t)-\pi\right) \tag{6.9}$$

$$V_4(t)=\frac{A_{RF}}{2}\cos\left(\Phi_{RF}(t)-\frac{3\pi}{4}\right)I(t)-\frac{A_{RF}}{2}\sin\left(\Phi_{RF}(t)-\frac{3\pi}{4}\right)Q(t)+\frac{A_{LO}}{2}\cos\left(\Phi_{LO}(t)-\frac{\pi}{2}\right) \tag{6.10}$$

$$V_5(t)=\frac{A_{RF}}{2}\cos\left(\Phi_{RF}(t)+\frac{3\pi}{4}\right)I(t)-\frac{A_{RF}}{2}\sin\left(\Phi_{RF}(t)+\frac{3\pi}{4}\right)Q(t)+\frac{A_{LO}}{2}\cos\left(\Phi_{LO}(t)-\frac{\pi}{2}\right) \tag{6.11}$$

$$V_6(t)=\frac{A_{RF}}{2}\cos\left(\Phi_{RF}(t)-\frac{\pi}{4}\right)I(t)-\frac{A_{RF}}{2}\sin\left(\Phi_{RF}(t)-\frac{\pi}{4}\right)Q(t)+\frac{A_{LO}}{2}\cos\left(\Phi_{LO}(t)-\pi\right) \tag{6.12}$$

For ideal power detectors, the output signal should be proportional to the square of the input signal. Suppose the power detectors in the six-port receiver have characteristic as follow:

$$P_{out}=\lambda P_{in}^{\,2} \tag{6.13}$$

Then the output signals of power detectors $V_{d3}(t) \sim V_{d6}(t)$ can be obtained as equation (6.14) – (6.17).

$$V_{d3}(t)=\lambda\left(\begin{array}{l}\frac{A_{RF}{}^2}{4}\left(\cos^2\left(\Phi_{RF}(t)-\frac{3\pi}{4}\right)I^2(t)+\sin^2\left(\Phi_{RF}(t)-\frac{3\pi}{4}\right)Q^2(t)\right)\\+\frac{A_{LO}{}^2}{4}\left(\frac{1+\cos(2\Phi_{LO}(t)-2\pi)}{2}\right)-\frac{A_{RF}{}^2}{4}\sin\left(2\Phi_{RF}(t)-\frac{3\pi}{2}\right)I(t)Q(t)\\+\frac{A_{RF}A_{LO}}{2}\cos\left(\Phi_{LO}(t)-\pi\right)\left(\cos\left(\Phi_{RF}(t)-\frac{3\pi}{4}\right)I(t)-\sin\left(\Phi_{RF}(t)-\frac{3\pi}{4}\right)Q(t)\right)\end{array}\right)$$

(6.14)

$$V_{d4}(t)=\lambda\left(\begin{array}{l}\frac{A_{RF}{}^2}{4}\left(\cos^2\left(\Phi_{RF}(t)-\frac{3\pi}{4}\right)I^2(t)+\sin^2\left(\Phi_{RF}(t)-\frac{3\pi}{4}\right)Q^2(t)\right)\\+\frac{A_{LO}{}^2}{4}\left(\frac{1+\cos(2\Phi_{LO}(t)-\pi)}{2}\right)-\frac{A_{RF}{}^2}{4}\sin\left(2\Phi_{RF}(t)-\frac{3\pi}{2}\right)I(t)Q(t)+\\\frac{A_{RF}A_{LO}}{2}\cos\left(\Phi_{LO}(t)-\frac{\pi}{2}\right)\left(\cos\left(\Phi_{RF}(t)-\frac{3\pi}{4}\right)I(t)-\sin\left(\Phi_{RF}(t)-\frac{3\pi}{4}\right)Q(t)\right)\end{array}\right)$$

(6.15)

$$V_{d5}(t)=\lambda\left(\begin{array}{l}\frac{A_{RF}{}^2}{4}\left(\cos^2\left(\Phi_{RF}(t)+\frac{3\pi}{4}\right)I^2(t)+\sin^2\left(\Phi_{RF}(t)+\frac{3\pi}{4}\right)Q^2(t)\right)\\+\frac{A_{LO}{}^2}{4}\left(\frac{1+\cos(2\Phi_{LO}(t)-\pi)}{2}\right)-\frac{A_{RF}{}^2}{4}\sin\left(2\Phi_{RF}(t)+\frac{3\pi}{2}\right)I(t)Q(t)+\\\frac{A_{RF}A_{LO}}{2}\cos\left(\Phi_{LO}(t)-\frac{\pi}{2}\right)\left(\cos\left(\Phi_{RF}(t)+\frac{3\pi}{4}\right)I(t)-\sin\left(\Phi_{RF}(t)+\frac{3\pi}{4}\right)Q(t)\right)\end{array}\right)$$

(6.16)

$$V_{d6}(t)=\lambda\left(\begin{array}{l}\frac{A_{RF}{}^2}{4}\left(\cos^2\left(\Phi_{RF}(t)-\frac{\pi}{4}\right)I^2(t)+\sin^2\left(\Phi_{RF}(t)-\frac{\pi}{4}\right)Q^2(t)\right)\\+\frac{A_{LO}{}^2}{4}\left(\frac{1+\cos(2\Phi_{LO}(t)-2\pi)}{2}\right)-\frac{A_{RF}{}^2}{4}\sin\left(2\Phi_{RF}(t)-\frac{\pi}{2}\right)I(t)Q(t)+\\\frac{A_{RF}A_{LO}}{2}\cos\left(\Phi_{LO}(t)-\pi\right)\left(\cos\left(\Phi_{RF}(t)-\frac{\pi}{4}\right)I(t)-\sin\left(\Phi_{RF}(t)-\frac{\pi}{4}\right)Q(t)\right)\end{array}\right)$$

(6.17)

After the low-pass filters, the high frequency section of the signals is blocked, therefore the output signals of the low-pass filters $V_{df3}(t) \sim V_{df6}(t)$ can be obtained:

$$V_{df3}(t)=\lambda\left(\frac{A_{RF}{}^2}{8}\left(I^2(t)+Q^2(t)\right)+\frac{A_{LO}{}^2}{8}+\frac{A_{RF}A_{LO}}{4}\left(\begin{array}{l}I(t)\cos\left(\Phi_{LO}(t)-\Phi_{RF}(t)-\frac{\pi}{4}\right)\\+Q(t)\sin\left(\Phi_{LO}(t)-\Phi_{RF}(t)-\frac{\pi}{4}\right)\end{array}\right)\right)$$

(6.18)

$$V_{df4}(t)=\lambda\left(\frac{A_{RF}{}^2}{8}\left(I^2(t)+Q^2(t)\right)+\frac{A_{LO}{}^2}{8}+\frac{A_{RF}A_{LO}}{4}\left(\begin{array}{l}I(t)\cos\left(\Phi_{LO}(t)-\Phi_{RF}(t)+\frac{\pi}{4}\right)\\+Q(t)\sin\left(\Phi_{LO}(t)-\Phi_{RF}(t)+\frac{\pi}{4}\right)\end{array}\right)\right)$$

(6.19)

$$V_{df5}(t)=\lambda\left(\frac{A_{RF}{}^2}{8}\left(I^2(t)+Q^2(t)\right)+\frac{A_{LO}{}^2}{8}+\frac{A_{RF}A_{LO}}{4}\begin{pmatrix}I(t)\cos\left(\Phi_{LO}(t)-\Phi_{RF}(t)-\frac{5\pi}{4}\right)\\+Q(t)\sin\left(\Phi_{LO}(t)-\Phi_{RF}(t)-\frac{5\pi}{4}\right)\end{pmatrix}\right)$$

(6.20)

$$V_{df6}(t)=\lambda\left(\frac{A_{RF}{}^2}{8}\left(I^2(t)+Q^2(t)\right)+\frac{A_{LO}{}^2}{8}+\frac{A_{RF}A_{LO}}{4}\begin{pmatrix}I(t)\cos\left(\Phi_{LO}(t)-\Phi_{RF}(t)-\frac{3\pi}{4}\right)\\+Q(t)\sin\left(\Phi_{LO}(t)-\Phi_{RF}(t)-\frac{3\pi}{4}\right)\end{pmatrix}\right)$$

(6.21)

When the power and frequency of the RF and LO signals are the same, then:

$$A_{RF}=A_{LO}=A,\ \omega_{RF}=\omega_{LO}$$

Set $\varphi_{LO}=\varphi_{RF}+\frac{\pi}{4}$, the output signals of the low-pass filters can be obtained as:

$$V_{df3}(t)=\lambda\frac{A^2}{8}\left(I^2(t)+Q^2(t)+2I(t)+1\right) \quad (6.22)$$

$$V_{df4}(t)=\lambda\frac{A^2}{8}\left(I^2(t)+Q^2(t)+2Q(t)+1\right) \quad (6.23)$$

$$V_{df5}(t)=\lambda\frac{A^2}{8}\left(I^2(t)+Q^2(t)-2I(t)+1\right) \quad (6.24)$$

$$V_{df6}(t) = \lambda \frac{A^2}{8}\left(I^2(t) + Q^2(t) - 2Q(t) + 1\right) \tag{6.25}$$

From (6.22) – (6.25), we have:

$$2\left(V_{df3}(t) - V_{df5}(t)\right) = \lambda A^2 I(t) \tag{6.26}$$

$$2\left(V_{df4}(t) - V_{df6}(t)\right) = \lambda A^2 Q(t) \tag{6.27}$$

From (6.26) and (6.27), *I(t)* and *Q(t)* can be obtained as:

$$I(t) = \frac{2\left(V_{df3}(t) - V_{df5}(t)\right)}{\lambda A^2} \tag{6.28}$$

$$Q(t) = \frac{2\left(V_{df4}(t) - V_{df6}(t)\right)}{\lambda A^2} \tag{6.29}$$

6.3 Six-port calibration

All of the above is the theoretical operating principle of the six-port receiver. From (6.28) and (6.29), λ and A are needed for six-port demodulation. For a real six-port receiver system, usually we do not have $A_{RF} = A_{LO} = A$. In this case, a calibration procedure is needed to obtain I and Q. Besides, a calibration of the six-port circuit can also minimize circuit and system errors.

Among many algorithms which have been proposed for the calibration of six-port reflectometers (SPR's) [19], Engen's six-port-to-four-port reduction [40], [41] seems to be one of the most attractive choices. This procedure determines the dependencies between the different power meter readings, yielding five real-valued reduction parameters which can be used to transform the SPR into a virtual four-port. No known standards are required for this reduction. The value measured by the virtual four-port is related to the reflection coefficient of the DUT by a so-called "error box" transformation. The three complex parameters of this transformation may be found by using one of the many existing methods for the calibration of traditional network analyzers.

6.3.1 W-plane calibration

Using the same notation as Stumper [42], the six-port to four-port reduction is given by the equations

$$p_1 = |w|^2 \tag{6.30}$$

$$Zp_2 = |w - w_1|^2 \tag{6.31}$$

$$Rp_3 = |w - w_2|^2 \tag{6.32}$$

where w is the complex reflection coefficient at the input of the imaginary ideal four-port reflectometer and the p_i denotes the power values p_1 to p_3, which are obtained from SPR measurements. Normally, good initial estimates of the five parameters are needed

for measurement at the ports labelled 1 to 3, normalized with respect to the power value measured at the reference port 4 of the SPR. The five reduction parameters to be determined by the calibration are the values of the real positive variables Z, R, and w_1, and the real and imaginary parts of the complex variable w_2.

The variable may be eliminated from equation (6.30) to (6.32) yielding the following nonlinear constraint equation:

$$\begin{aligned} & Ap_1^{\,2} + BZ^2P_2^{\,2} + CR^2P_3^{\,2} + (C-A-B)ZP_1P_2 \\ & + (B-C-A)RP_1P_3 + (A-B-C)ZRP_2P_3 \\ & + A(A-B-C)P_1 + B(B-C-A)ZP_2 \\ & + C(C-A-B)RP_3 + ABC = 0 \end{aligned} \tag{6.33}$$

where

$$A = |w_1 - w_2|^2 \tag{6.34}$$

$$B = |w_2|^2 \tag{6.35}$$

Equation (6.33) can be solved by measuring at least nine (usually 13 in practice) arbitrary different terminations. The solution of (6.33) [*A, B, C, Z, R*] allows transformation of a six-port to a perfect four-port reflectometer in a notional "W" complex plane. The W-plane reflection coefficient is

$$W = \frac{p_1 - Z^2 q_2 + C}{2\sqrt{C}} + j\frac{[C(A+B-C)+(A-B+C)p_1 - (A-B-C)Z^2 p_2 - 2CR^2 p_3}{\pm 2\sqrt{C(2AB+2BC+2AC-A^2-B^2-C^2)}} \tag{6.36}$$

6.3.2 Error-box calibration

A two-port error box is inserted between the notional four-port and the DUT so that the virtual reflection reading from the notional perfect reflectometer obtained by W-plane calibration are transferred to the real reflection coefficients Γ. This is done through a bilinear transformation

$$\Gamma = \frac{e - W}{cW - d} \tag{6.37}$$

where c, d and e are complex constants related to the S-parameters of the error box

$$c = -S_{22}$$

$$d = S_{12}S_{21} - S_{11}S_{22}$$

$$e = S_{11}$$

W-plane to Γ-plane bilinear transformation is shown in Figure 6.4.

After six-port-to-four-port reduction and error box calibration, $|b_2|$ and Γ can be determined. Therefore, the amplitude ratio and the phase difference of a1 and a_2 can be obtained.

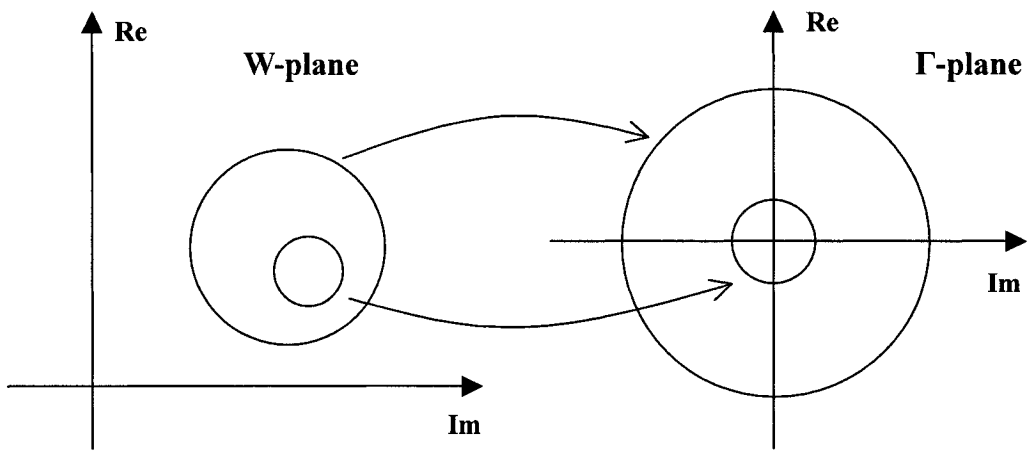


Figure 6.4 W-plane to Γ-plane bilinear transformation

6.3.3 Real-time calibration

Physical six-port calibration method uses external physical standard terminals connected to its input port. However, for a wireless receiver, it would be entirely impractical. It is therefore necessary to develop another calibration method that is free of any external connection.

As we know, the leakage of the received signal to the local oscillator reference port is small, and may be neglected. In this case, the relationship between the output data of SPR and the three power ratios of the detectors become linear, and can be expressed as follow:

$$\Gamma_r = A_{r1}p_1 + A_{r2}p_2 + A_{r3}p_3 + C_r \tag{6.38}$$

$$\Gamma_i = A_{i1}p_1 + A_{i2}p_2 + A_{i3}p_3 + C_i \tag{6.39}$$

where Γ_r, Γ_i are the calculated output data, whereas A_{rj}, A_{ij} (j = *1, 2, 3*) and C_r, C_i are calibration parameters to be determined. p_1, p_2, p_3 are the power ratios of the output detectors of the six-port.

From the equations above, it is clear that a total of eight parameters A_{r1}, A_{r2}, A_{r3}, A_{j1}, A_{j2} A_{j3} and C_r, C_i should be determined from the calibration procedure. Therefore, four known sets of *I*, *Q* values or signal standards (SS) should be used to obtain eight linear equations for the solution of the above eight parameters. These four known sets of *I*, *Q* values are ideally selected as being the four different states of modulated signals, for example, 4 different states of QPSK or QAM16 signals. However, simulation shows that the calculation diverges when the four known sets of I, Q values have the same amplitude. Hence, at least one signal standard should have amplitude different from the remaining three. Therefore, for QPSK, we could choose three sets of I, Q values from the four states of a QPSK signal and a zero signal at the input of the receiver as the

fourth known I, Q set. The zero signal input can be achieved by applying a large bias to drive the low-noise amplifier (LNA) of the receiver far beyond cut-off. An alternative method is to insert an attenuation in the fourth set of the QPSK signal.

From the four sets of I, Q values above or signal standards, we have four sets of detector output power ratios of the six-port, namely, Q_{kj} with k = 1, 2, 3, 4 and j = 1, 2, 3. Substituting Q_{kj} into Equation (6.37) and equating the left-hand side of these equations to the standard I, Q values (1, 1), (-1, 1), (-1, -1), and (0, 0), we have two systems of four linear equations. One of them corresponds to Equation (6.38), and the other to Equation (6.39). Solving these sets of linear equations, the parameters, A_{rj} , A_{ij} j = (1, 2, 3) and C_r, C_i can be obtained, and the calculations of the receiver output I, Q data can be made using the ratios of the output readings of the power detectors in Equation (6.38) and (6.39).

6.4 Simplified demodulation algorithm for BPSK, QPSK schemes

As mentioned before, except for universal demodulation algorithm for six-port receiver that we discussed before, there are some special demodulation algorithms for certain modulation schemes (such as BPSK, QPSK). In this case, the calibration procedure can be omitted.

Considering the SIW six-port circuit proposed in Chapter 5 (see Figure 6.2), define the input signal from port 1 as $\vec{a} = ae^{j(wt+\phi_a)}$ and the input signal from port 2 as $\vec{b} = be^{j(wt+\phi_b)}$, the output power of the four output ports (before power detectors) as *p3*, *p4*, *p5*, *p6* and the output voltages of the power detectors *as P3*, *P4*, *P5*, *P6*. We have,

$$p3 = 0.5(\vec{a}e^{-j180^\circ} + \vec{b}e^{-j135^\circ}) \tag{6.40}$$

$$p4 = 0.5(\vec{a}e^{-j90^\circ} + \vec{b}e^{-j135^\circ}) \tag{6.41}$$

$$p5 = 0.5(\vec{a}e^{-j90^\circ} + \vec{b}e^{j135^\circ}) \tag{6.42}$$

$$p6 = 0.5(\vec{a}e^{-j180^\circ} + \vec{b}e^{-j45^\circ}) \tag{6.43}$$

$$P3 = p3 * p3^* \tag{6.44}$$

$$P4 = p4 * p4^* \tag{6.45}$$

$$P5 = p5 * p5^* \tag{6.46}$$

$$P6 = p6 * p6^* \tag{6.47}$$

If $\vec{b}$ is a BPSK signal, $\vec{b} = be^{jwt}\{e^{j90^\circ}, e^{j270^\circ}\}$ and $\vec{a} = ae^{jwt}e^{j45^\circ}$ (reference signal). The power levels of these four ports should be:

State 1: $\vec{b} = be^{j(wt+90^\circ)}$ (Q= +1)

$$p3 = 0.5(ae^{-j135^\circ} + be^{-j45^\circ})e^{jwt}$$

$$p4 = 0.5(ae^{-j45^\circ} + be^{-j45^\circ})e^{jwt}$$

$$p5 = 0.5(ae^{-j45^\circ} + be^{-j135^\circ})e^{jwt}$$

$$p6 = 0.5(ae^{-j135^\circ} + be^{j45^\circ})e^{jwt}$$

$$P3 = 0.25(a^2 + b^2)$$

$$P4 = 0.25(a+b)^2$$

$$P5 = 0.25(a^2 + b^2)$$

$$P6 = 0.25(a-b)^2$$

As the amplitude of signal $\vec{a}$ and signal $\vec{b}$, a, b should be positive real numbers. So we have:

$$P4 > P3 = P5 > P6 \tag{6.48}$$

State 2: $\vec{b} = be^{j(wt+270^\circ)}$ (Q= -1)

$$p3 = 0.5(ae^{-j135^\circ} + be^{j135^\circ})e^{jwt}$$

$$p4 = 0.5(ae^{-j45^\circ} + be^{j135^\circ})e^{jwt}$$

$$p5 = 0.5(ae^{-j45^\circ} + be^{j45^\circ})e^{jwt}$$

$$p6 = 0.5(ae^{-j135^\circ} + be^{-j135^\circ})e^{jwt}$$

$$P3 = 0.25(a^2 + b^2)$$

$$P4 = 0.25(a^2 + b^2)$$

$$P5 = 0.25(a - b)^2$$

$$P6 = 0.25(a + b)^2$$

Same as (6.48), we have:

$$P6 > P3 = P4 > P5 \tag{6.49}$$

From (6.48) and (6.49) we find

$$\begin{cases} Q = +1 & (P6 > P5) \\ Q = -1 & (P6 < P5) \end{cases}$$

If $\vec{b}$ is a QPSK signal, $\vec{b} = be^{jwt}\{e^{j45^\circ}, e^{j135^\circ}, e^{j225^\circ}, e^{j315^\circ}\}$ and $\vec{a} = ae^{jwt}e^{j0^\circ}$ (reference signal), the power levels of these four ports should be:

State 1: $\vec{b} = be^{j(wt+45^\circ)}$ (I= +1, Q= +1)

$$p3 = 0.5(ae^{-j180^\circ} + be^{-j90^\circ})e^{jwt}$$

$$p4 = 0.5(ae^{-j90^\circ} + be^{-j90^\circ})e^{jwt}$$

$$p5 = 0.5(ae^{-j90^\circ} + be^{j180^\circ})e^{jwt}$$

$$p6 = 0.5(ae^{-j180^\circ} + be^{-j0^\circ})e^{jwt}$$

$$P3 = 0.25(a^2 + b^2)$$

$$P4 = 0.25(a+b)^2$$

$$P5 = 0.25(a^2 + b^2)$$

$$P6 = 0.25(a-b)^2$$

So we have:

$$P5 > P3 = P4 > P6 \tag{6.50}$$

State 2: $\vec{b} = be^{j(wt+135°)}$ (I= -1, Q= +1)

$$p3 = 0.5(ae^{-j180°} + be^{j0°})e^{jwt}$$

$$p4 = 0.5(ae^{-j90°} + be^{j0°})e^{jwt}$$

$$p5 = 0.5(ae^{-j90°} + be^{-j90°})e^{jwt}$$

$$p6 = 0.5(ae^{-j180°} + be^{j90°})e^{jwt}$$

$$P3 = 0.25(a-b)^2$$

$$P4 = 0.25(a^2 + b^2)$$

$$P5 = 0.25(a+b)^2$$

$$P6 = 0.25(a^2 + b^2)$$

We have:

$$P5 > P6 = P4 > P3 \tag{6.51}$$

State 3: $\vec{b} = be^{j(wt+225°)}$ (I= -1, Q= -1)

$$p3 = 0.5(ae^{-j180°} + be^{j90°})e^{jwt}$$

$$p4 = 0.5(ae^{-j90°} + be^{j90°})e^{jwt}$$

$$p5 = 0.5(ae^{-j90°} + be^{j0°})e^{jwt}$$

$$p6 = 0.5(ae^{-j180°} + be^{j180°})e^{jwt}$$

$$P3 = 0.25(a^2 + b^2)$$

$$P4 = 0.25(a-b)^2$$

$$P5 = 0.25(a^2 + b^2)$$

$$P6 = 0.25(a+b)^2$$

We have:

$$P6 > P5 = P3 > P4 \tag{6.52}$$

State 4: $\vec{b} = be^{j(wt+315°)}$ (I= +1, Q= -1)

$$p3 = 0.5(ae^{j180°} + be^{j180°})e^{jwt}$$

$$p4 = 0.5(ae^{-j90°} + be^{j180°})e^{jwt}$$

$$p5 = 0.5(ae^{-j90°} + be^{j90°})e^{jwt}$$

$$p6 = 0.5(ae^{-j180^\circ} + be^{-j90^\circ})e^{jwt}$$

$$P3 = 0.25(a+b)^2$$

$$P4 = 0.25(a^2 + b^2)$$

$$P5 = 0.25(a-b)^2$$

$$P6 = 0.25(a^2 + b^2)$$

We have:

$$P3 > P4 = P6 > P5 \tag{6.53}$$

From (6.50) to (6.53) we find

$$\begin{cases} I = +1 & (P3 > P6) \\ I = -1 & (P3 < P6) \\ Q = +1 & (P5 > P6) \\ Q = -1 & (P5 < P6) \end{cases}$$

From the above, the I-Q signal can be easily determined by comparing the voltages of the output signals. Therefore, for this kind of schemes, the DSP demodulation algorithms for the six-port receiver can be dramatically simplified.

CHAPTER VII

RECEIVER PERFORMANCE AND DEMODULATION RESULTS

7.1 Introduction

Within the operating frequency band of the receiver (22 GHz – 26 GHz), three modulation schemes (QPSK, QAM16, OFDM) are selected to test the performance of the proposed six-port software receiver for phase, amplitude, and frequency modulations. System level simulations are made using Agilent ADS and Matlab, and measured BER results of this new six-port SDR receiver are also presented. The simulated and measured results are based on the SIW six-port receiver.

7.2 System simulation of six-port SDR receiver platform

7.2.1 QPSK demodulation

To test the receiver performance, system level simulations are made based on ADS. The ADS simulation schematic for QPSK demodulation is given in Figure 7.1.

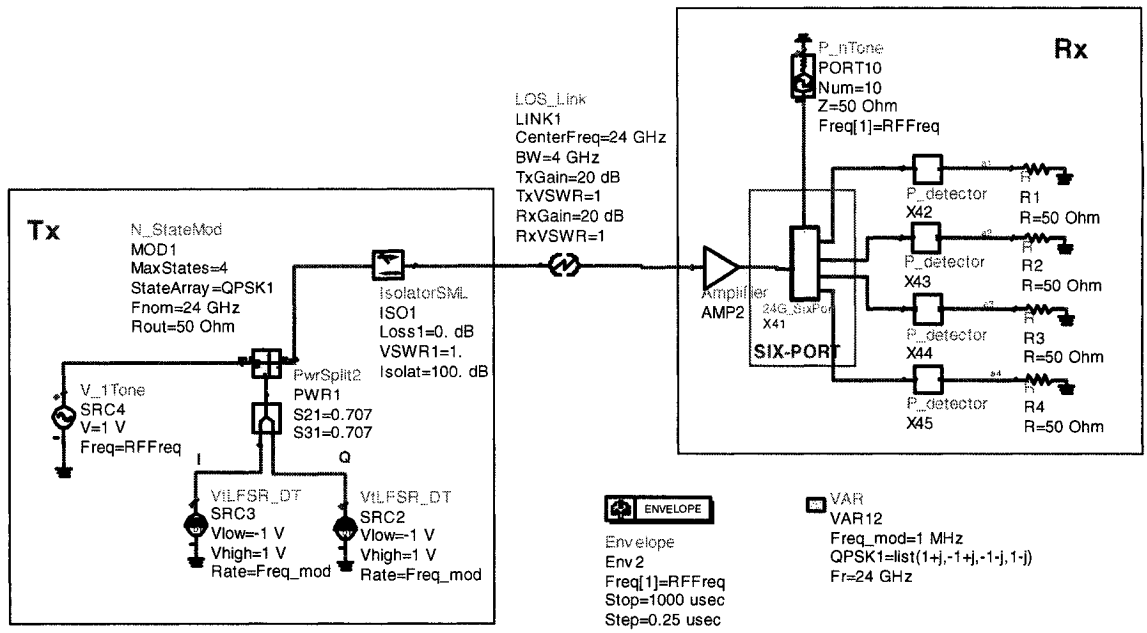


Figure 7.1 ADS simulation schematic for QPSK of six-port SDR receiver

The simulation system schematic consists of a transmitter, a propagation link and a six-port receiver. As shown in Figure 7.1, the transmitter is composed of a QPSK modulator with a pseudo-random bit sequence source. The six-port receiver consists of an SIW six-port circuit, four RF detectors, and four 50 Ohm terminals. In this simulation, the LO is supposed to be locked in phase. The propagation of RF the signal is simulated using the LOS_Link component, which is based on the model of Friis [43] and is provided by the components library of ADS software. The receiver is simulated at a frequency of 24 GHz, with 1 Mb/s bit rate, 4 dBm transmission power, -10 dBm LO power, 20 dB antennas gain. The distance of propagation is 100 m. Four sets of output signals from the 50 Ohm terminals are collected for DSP decode, which will be accomplished by Matlab.

Figure 7.2 demonstrates the simulated waveforms of the four output signals (after power detectors) of the six-port receiver. It can be seen that the output waveform is corresponded to the equation (6.18)- (6.21).

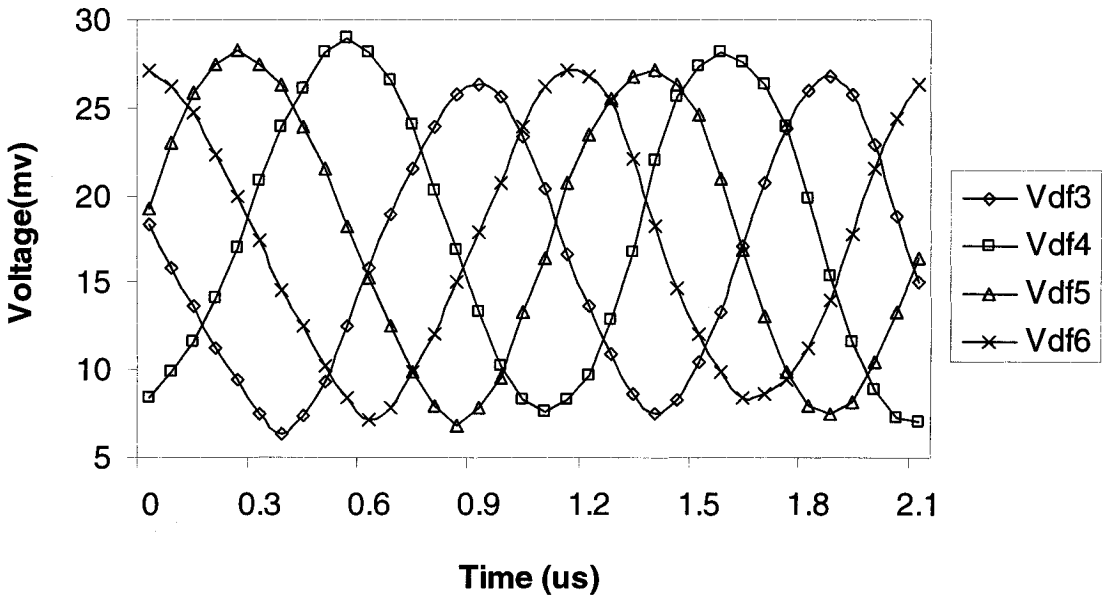


Figure 7.2 Waveform of the four output signals of the six-port

As we know, QPSK signal is a phase modulation signal with four different states (shown in Figure 7.3). As discussed in Chapter VI, after calibration, we can get the complex constants related to the six-port circuit X_i, Y_i which are required to calculate the output vector signal. Then the output signal can be demodulated by a suitable decision algorithm.

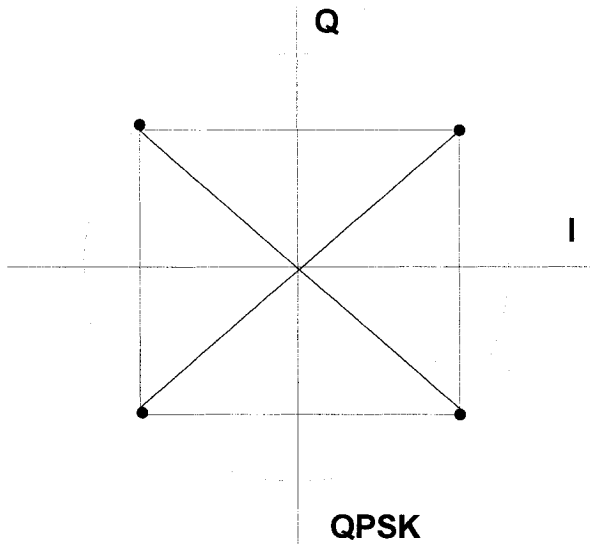


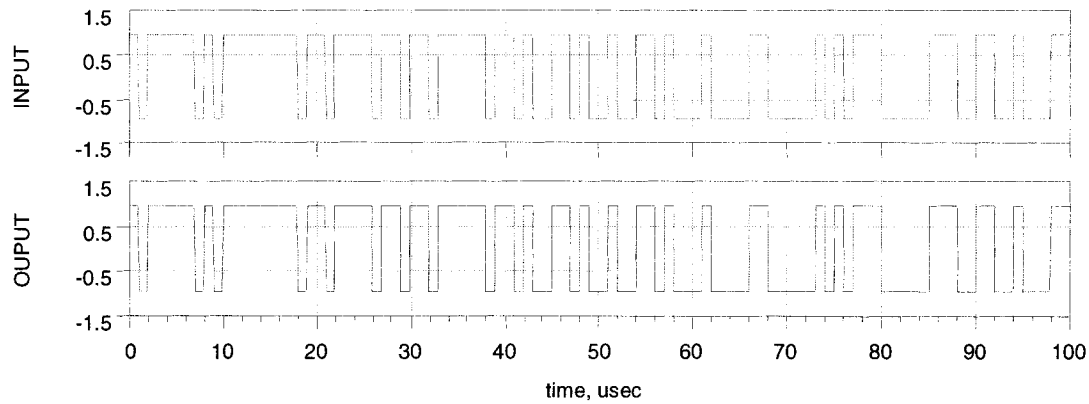
Figure 7.3 Signal constellations for QPSK modulation

Table 7.1 Demodulation results for QPSK signal

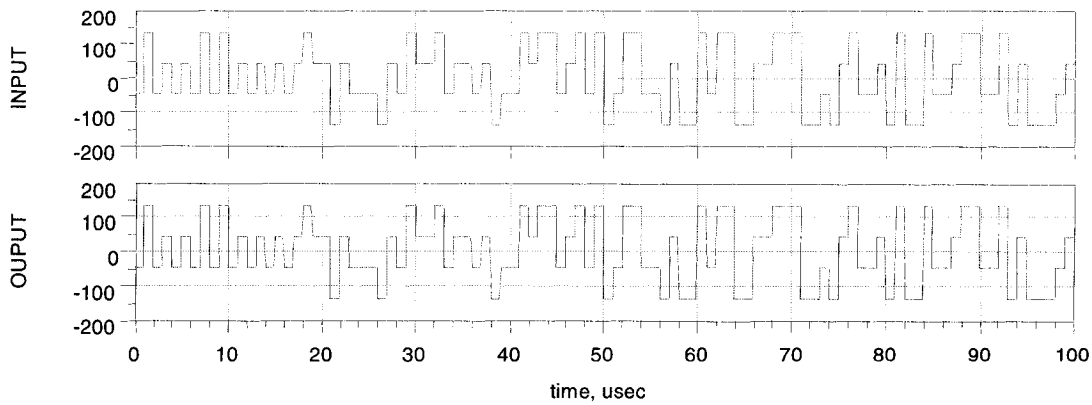
Input	Output
$1\angle 45°$	$1.0205\angle 46.66°$
$1\angle 135°$	$0.9595\angle 139.42°$
$1\angle 225°$	$1.0000\angle 224.68°$
$1\angle 315°$	$1.0365\angle 315.45°$

Table 7.1 shows the simulated demodulation results of the six-port receiver for QPSK modulations (P_{LO} = -15dBm, P_{RF} = -20dBm). The simulated demodulation results show that the receiver has an accuracy of ± 5 degrees in phase and ± 0.2 dB in amplitude for QPSK modulation.

The input and output waveforms and phases of QPSK are shown in Figure 7.4. The INPUT is a pseudo-random bit sequence QPSK signal. The OUTPUT is the signal obtained signal at the output port of the receiver. It can be seen that the output signals (demodulation signals) are exactly the same as the input signals, which confirms the operating principle of the receiver.

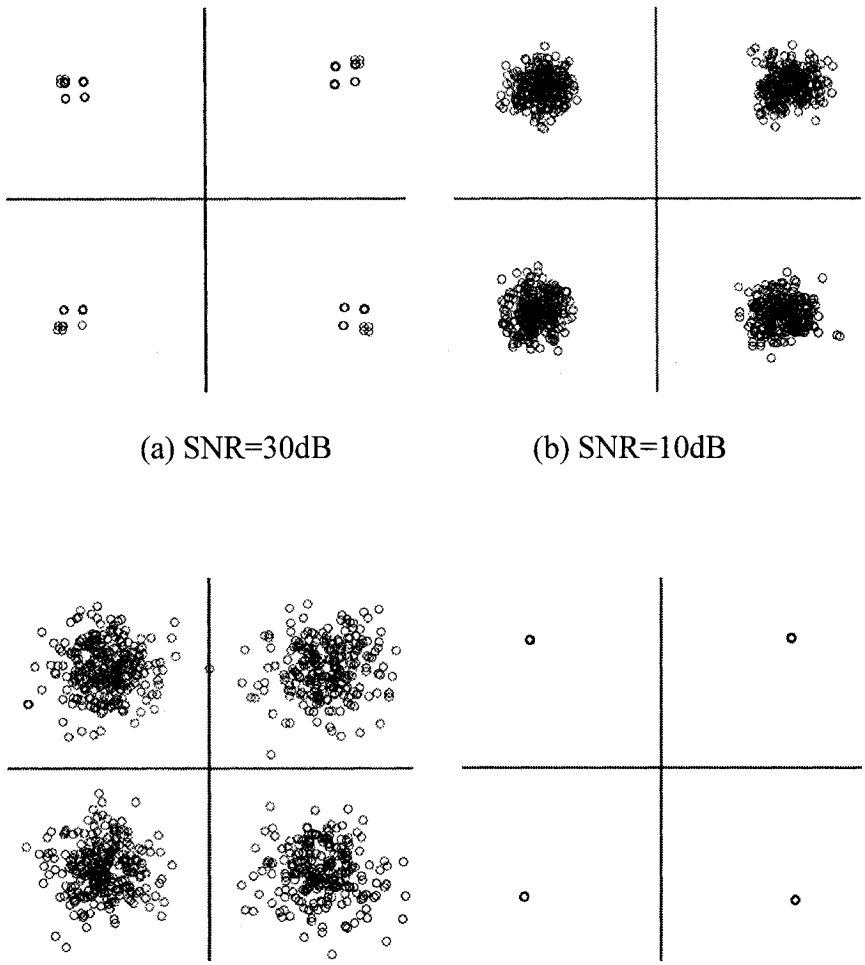


(a) Input and output waveforms as a function of time



(b) Input and output phases as a function of time

Figure 7.4 Simulated demodulation results of QPSK modulation

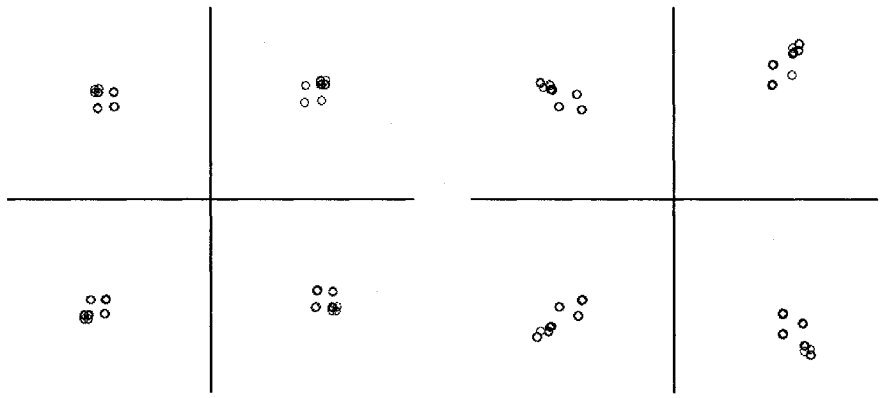


(a) SNR=30dB (b) SNR=10dB

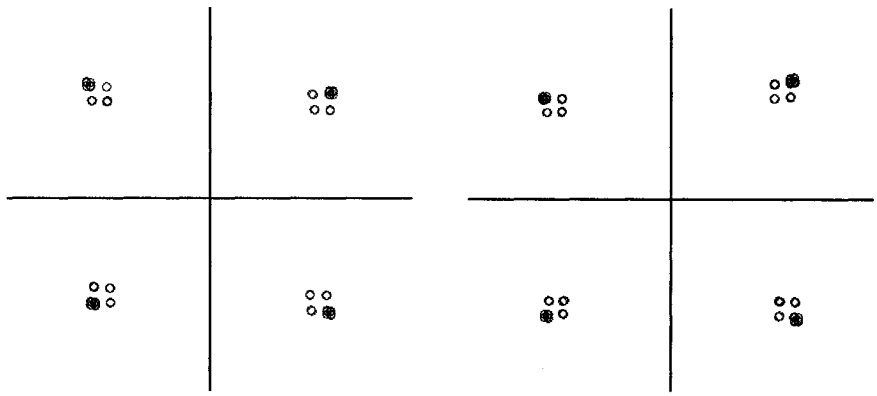
(c) SNR=4dB (d) Demodulation result

Figure 7.5 Simulated output signal constellations of QPSK with different SNRs

Figure 7.5 shows the simulated output QPSK signal constellations for various signal-to-noise ratios (SNR). A Gaussian white noise is added to the input signal and the output signal constellations are presented in Figure 7.5 (a)–(c) for QPSK with SNR equal to 30, 10, and 4 dB respectively. Demodulation results after the decision algorithm are presented in Figure 7.5(d).



(a) RF=-20dBm LO=-10dBm (b) RF=-20dBm LO=-20dBm



(c) RF=-30dBm LO=-10dBm (d) RF=-30dBm LO=-20dBm

Figure 7.6 Simulated output signal constellations for QPSK for different RF and LO power levels

Figure 7.6 shows the simulated output signal constellations for QPSK with different RF and LO power levels, the power levels of RF and LO are changed from –10 dBm to –30dBm. By defining the demodulation error as follows:

$$Error = \frac{|output\_signal - input\_signal|}{|input\_signal|} \tag{7.1}$$

we find that when the LO power level is bigger than the RF power level, the highest error is under 5%; when the LO power level is the same as the RF power level, the highest error is about 15%. It indicates that in order to reduce the error of QPSK demodulation, the power level of LO should be bigger than the power level of RF input.

7.2.2 QAM16 demodulation

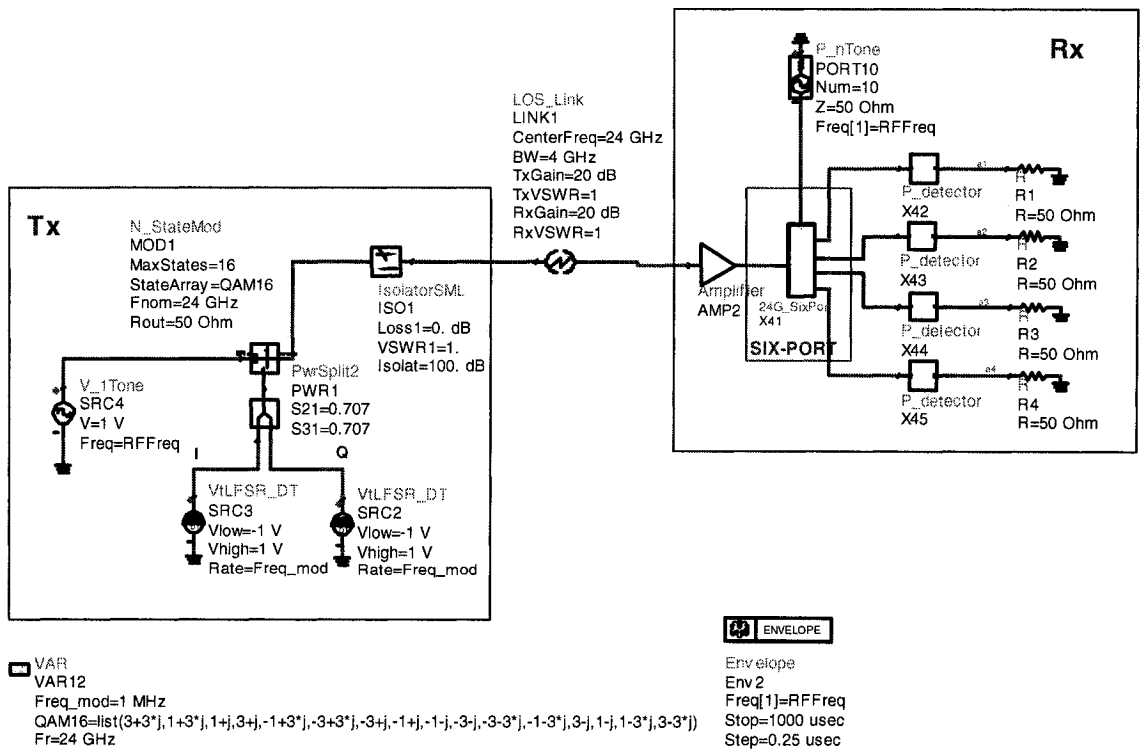


Figure 7.7 ADS simulation schematic for QAM16 of six-port SDR receiver

For QAM16 modulation, we also use ADS to do the system simulation. The ADS simulation schematic for QAM16 demodulation is given in Figure 7.7.

Unlike QPSK, QAM16 signal is a phase-amplitude modulation signal with 16 different states (shown in Figure 7.8). Table 7.2 shows the simulated demodulation results for QAM16 modulations. (P_{LO} = -15 dBm, P_{RF} = -20dBm)

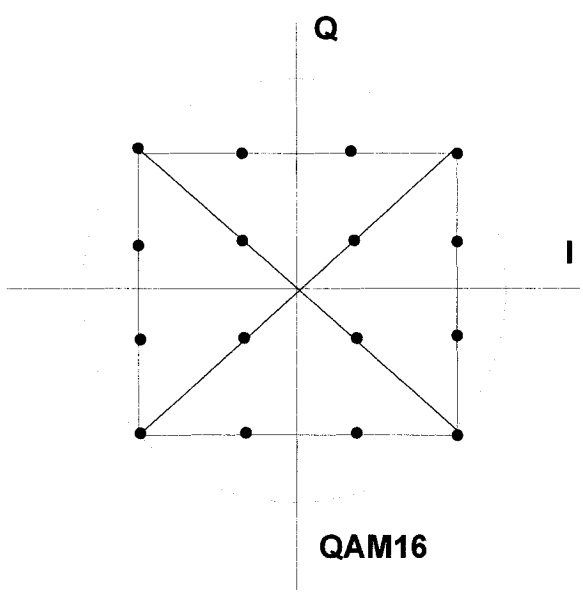


Figure 7.8 Signal constellations for QAM16 modulation

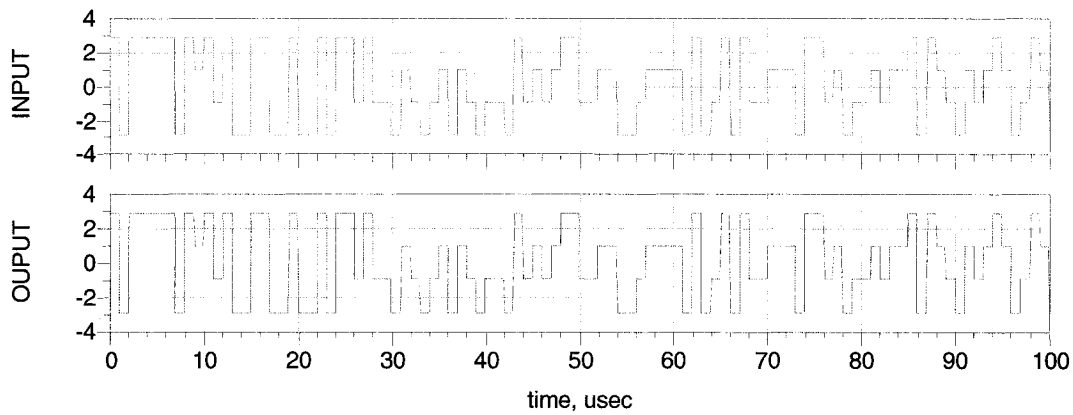
The simulated demodulation results show that the receiver has an accuracy of ± 5 degrees in phase and ± 0.4 dB in amplitude for QAM16 signals.

Table 7.2 Demodulation results for QAM16 signals

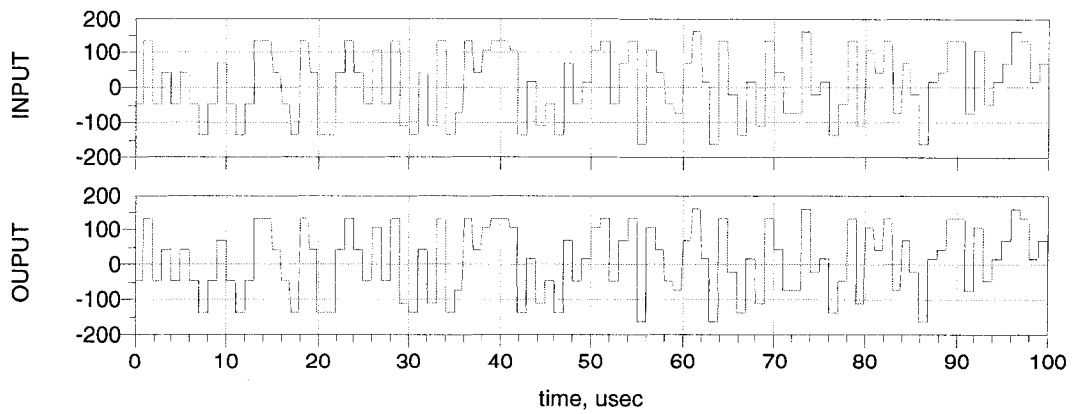
Input	Output
4.2426∠45°	4.1636∠47.46°
3.1623∠18.43°	3.1548∠18.90°
1.4142∠45°	1.2892∠43.18°
3.1623∠71.56°	2.9562∠73.15°
3.1623∠341.57°	3.2395∠341.25°
4.2426∠315°	4.3099∠314.82°
3.1623∠288.44°	3.1222∠287.17°
1.4142∠315°	1.4511∠311.64°
1.4142∠225°	1.5123∠227.20°
3.1623∠251.56°	3.1305∠249.71°
4.2426∠225°	4.2693∠224.02°
3.1623∠198.43°	3.1952∠201.29°
3.1623∠108.44°	2.9198∠111.52°
1.4142∠145°	1.2758∠143.24°
3.1426∠161.57°	3.0527∠166.60°
4.2426∠145°	3.9331∠141.67°

The input and output waveforms and phases of QAM16 are shown in Figure 7.9. The INPUT is a pseudo-random bit sequence QAM16 signal. The OUTPUT is the signal obtained at the output port of the receiver. It can be seen that the output signals (demodulation signals) are exactly the same as the input signals.

Figure 7.10 shows the simulated output QAM16 signal constellations for various SNR. A Gaussian white noise is added to the input signal and the output signal constellations are presented in Figure 7.10 (a)–(c) for QAM16 signal with SNR equal 30-, 15-, and 8-dB respectively. Demodulation results after the decision algorithm are presented in Figure 7.10(d).

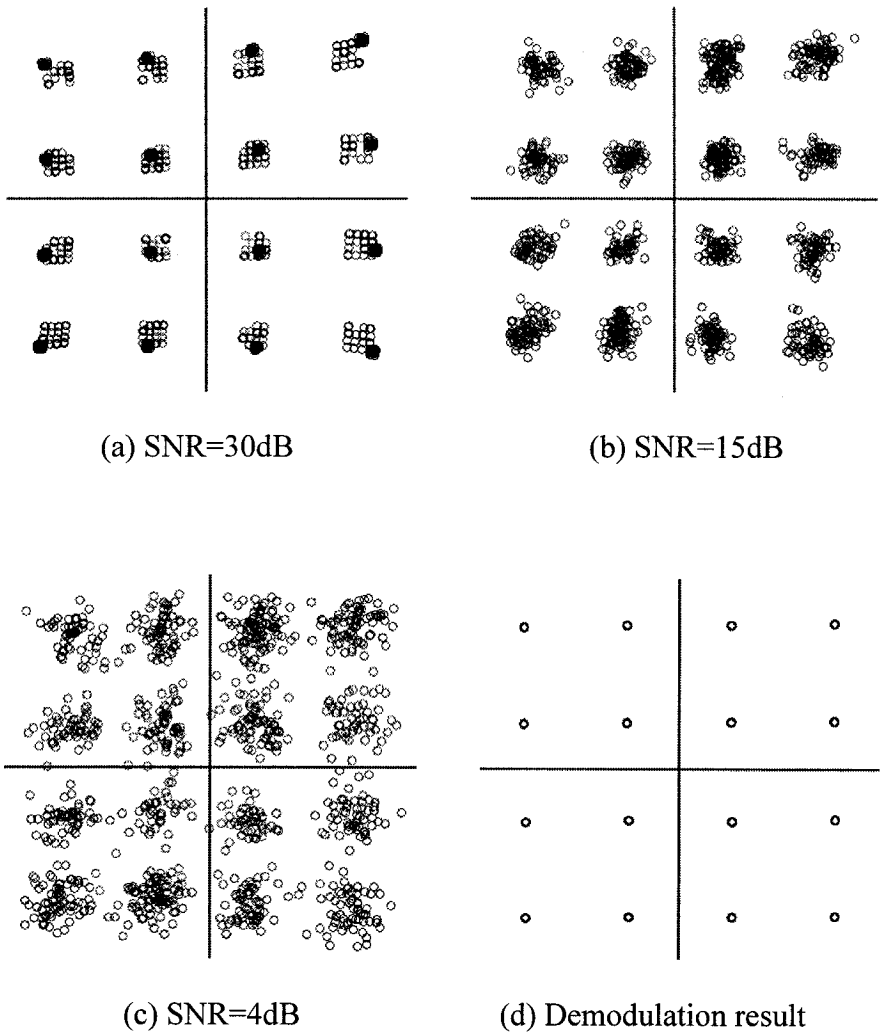


(a) Input and output waveforms as a function of time



(b) Input and output phases as a function of time

Figure 7.9 Simulated demodulation results for QAM16



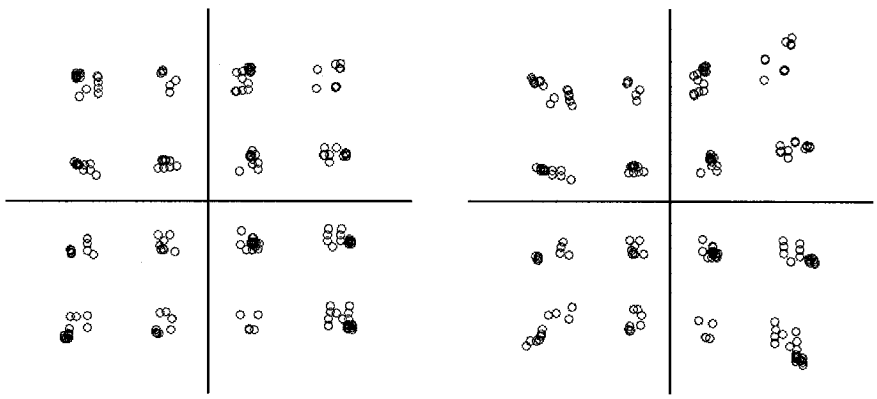
(a) SNR=30dB (b) SNR=15dB

(c) SNR=4dB (d) Demodulation result

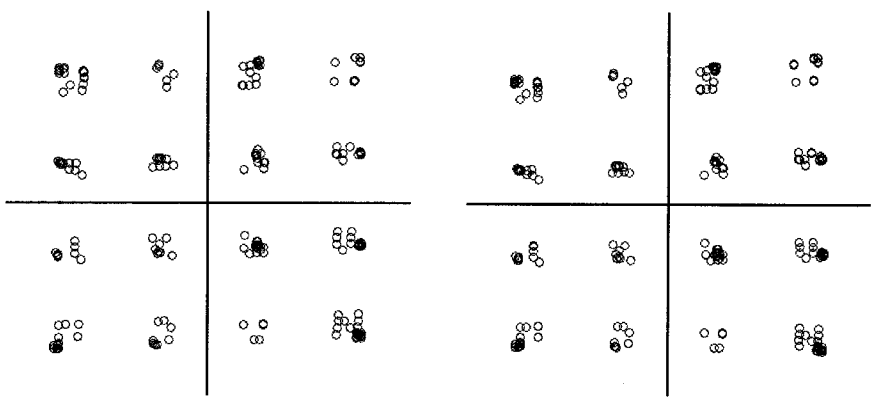
Figure 7.10 Simulated output signal constellations for QAM16 with different SNRs.

Figure 7.11 shows the simulated output signal constellations for QAM16 with different RF and LO power levels, the power levels of RF and LO are changed from –10 dBm to –30dBm. When the LO power level is bigger than the RF power level, the highest error (as defined in Equation 7.1) is under 5%; when the LO power level is same as the RF

power level, the highest error is about 17%. Therefore, to reduce the error of QAM16 demodulation, the power level of LO should be bigger than the power level of the RF input.



(a) RF=-20dBm LO=-10dBm (b) RF=-20dBm LO=-20dBm



(c) RF=-30dBm LO=-10dBm (d) RF=-30dBm LO=-20dBm

Figure 7.11 Simulated output signal constellations for QAM16 with different RF and LO power levels

7.2.3 OFDM demodulation

Over the past few years, orthogonal frequency division multiplexing (OFDM) has received considerable attention from the general wireless community in particular from the wireless LAN (WLAN) standards groups. Groups such as IEEE 802.11a and ETSI BRAN have selected OFDM as the best waveform for providing reliable high data rates for WLANs.

OFDM is intrinsically able to handle the most common distortions found in the wireless environment without requiring complex receiver algorithms. As it turns out, the wireless environment and, in particular, the WLAN environment presents a harsh channel for communications. Conventional modulation methods suffer from multi-path in both the frequency domain and the time domain. In the frequency domain, multi-path causes groups of frequencies to be attenuated and shifted in phase which severely distorts the symbols. In the time domain, multi-path basically smears adjacent symbols into each other. Many typical systems overcome these problems with expensive adaptive filters. OFDM, on the other hand, uses groups of narrowband signals to pierce through this environment and employs a guard interval between symbols in order to counter the inherent time domain smearing. This allows OFDM systems to use lower complexity receivers and still maintain robust performance. In short, OFDM is a popular choice

because of its robust performance in multi-path without the need for complex receiver algorithms.

As a modulation scheme, OFDM has both advantages and disadvantages; however, in many of the modern wireless applications, the disadvantages of OFDM can be overcome with careful design choices. Consequently, OFDM is frequently the best optimizing cost solution for wireless environments (like WLAN's) where multi-path is the primary impairment to reliable communications.

An OFDM signal is basically a bundle of narrowband carriers transmitted in parallel at different frequencies from the same source. This modulation scheme is often labelled as a "multi-carrier" scheme as opposed to conventional "single carrier" schemes.

Each individual carrier, commonly called a sub-carrier, transmits information by modulating the phase or the amplitude of the sub-carrier over the symbol duration. That is, each sub-carrier uses either phase-shift-keying (PSK) or quadrature-amplitude-modulation (QAM) to send information just as conventional single carrier systems. However, OFDM or multi-carrier systems use a large number of low symbol rate sub-carriers. The spacing between these sub-carriers is selected to be the inverse of the symbol duration so that each sub-carrier is orthogonal or non-interfering. This is the smallest frequency spacing that can be used without creating interference.

At first glance it might appear that OFDM systems must modulate and demodulate each sub-carrier individually. Fortunately, the well-known fast Fourier transform (FFT) provides a highly efficient method for modulating and demodulating these parallel sub-carriers as a group rather than individually.

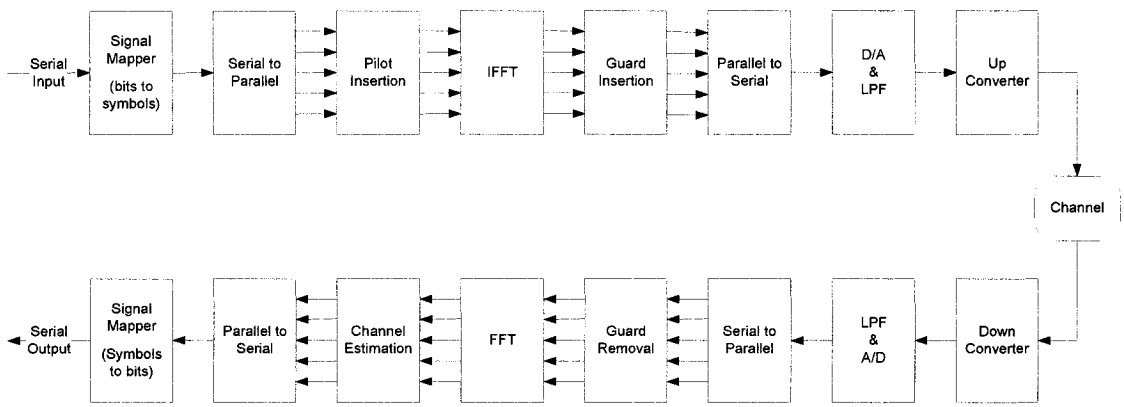


Figure 7.12 System architecture of FFT-based OFDM system

Figure 7.12 illustrates the process of a typical FFT-based OFDM system. The incoming serial data is first grouped and mapped by different mapping schemes saved in "signal mapper". Then the signals are converted from serial to parallel to prepare different data groups for different OFDM sub-carriers. After inserting pilots either to all sub-carriers with a specific or uniform period between the information data sequence, an IFFT block is used to transform the data sequence into a time domain signal. A guard interval is inserted between symbols to avoid intersymbol interference (ISI) caused by multi-path distortion. The discrete symbols are converted into analog and low-pass filtered for RF

up-conversion. The receiver performs the inverse process of the transmitter, after down-conversion, the signals are transferred to the discrete domain through ADC and low pass filter, the guard interval is removed and the signals are fed to a FFT block. Following the FFT block, the pilot signals are extracted and the estimated channel for the data sub-channels is obtained in channel the estimation block. Finally, the binary data is obtained after the "signal mapper" block.

To test the receiver performance, Matlab-Simulink software is used for the system level simulation. The Simulink model for OFDM demodulation simulation is shown in Figure 7.13

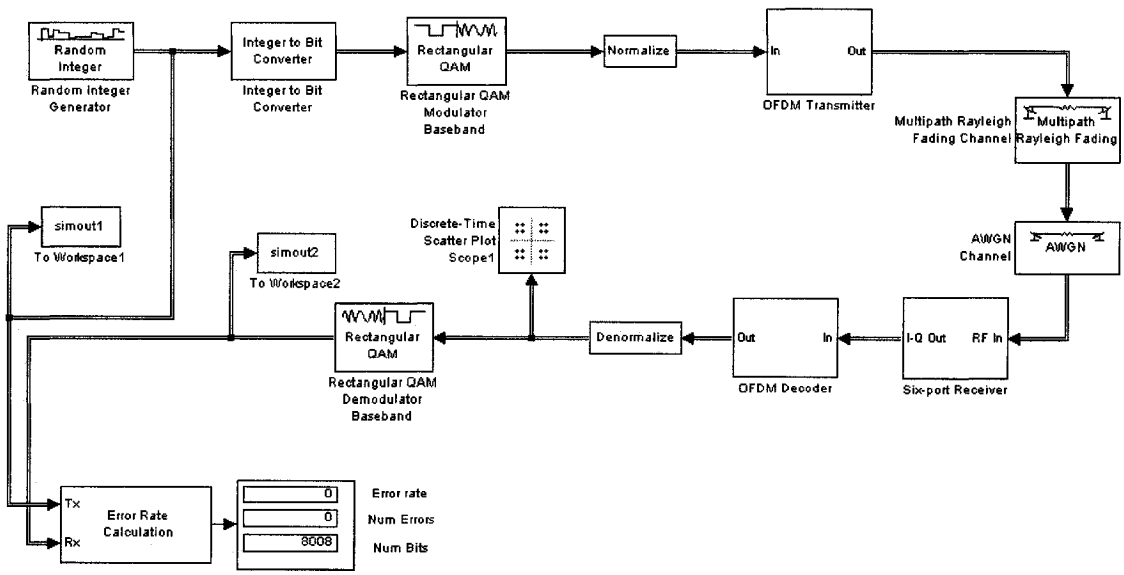


Figure 7.13 Simulink model for OFDM modulation/ demodulation

The simulation is applied with 32 active sub-carriers, QAM16 signal is selected as the modulation scheme for each sub-carriers. The signal propagation channel is simulated using additive white Gaussian noise (AWGN) channel model and multi-path Rayleigh fading channel model, which are provided by the components library of Simulink. software. The simulation parameters are listed in Table 7.3.

Table 7.3 Simulation parameters of OFDM demodulation

Parameter	**Specifications**
Number of Sub-carrier	32
Sub-channel modulation scheme	16QAM
data rate of OFDM signal	1Mbps / sub-carrier
Transmitter power	0 dBm
Local oscillator power	0 dBm
FFT Size	256
Pilot Ratio	1/8
Guard Type	Cyclic Extension
Guard Interval	64
Channel Model	AWGN, multi-path Rayleigh fading

Figure 7.15 shows the simulated output signal constellations for OFDM corresponding to the signals "(a)", "(b)", "(c)" and "(d)" in Figure 7.14. Figure 7.15 (a) is the output signal after six-port computation. Due to the IFFT transform and transmission channel distortions, the signal constellations are not fixed, and in fact, the signal constellations are almost random. Figure 7.15 (b) shows the output signal after guard removal and FFT. It can be seen that the signals are distorted by multi-path fading. The signals after distortion recovery and QAM demodulation output (after decision algorithms) are shown in Figure 7.15 (c) and Figure 7.15 (d), respectively. That signals are recovered quite well in the constellation set.

The simulated input and output waveforms of six-port receiver for OFDM are shown in Figure 7.16. The input is a pseudo-random 4-bit integer sequence. The output is the demodulation signal obtained at the output port of the receiver where the SNR level is 30 dB. It can be seen that the output signals (demodulated signals) are exactly the same as the input signals.

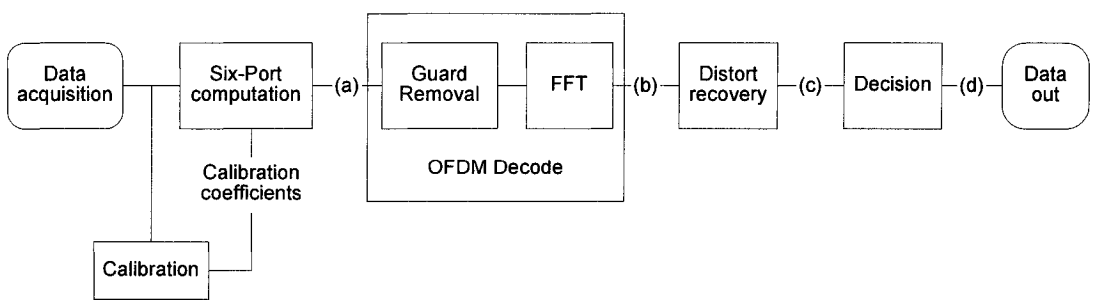
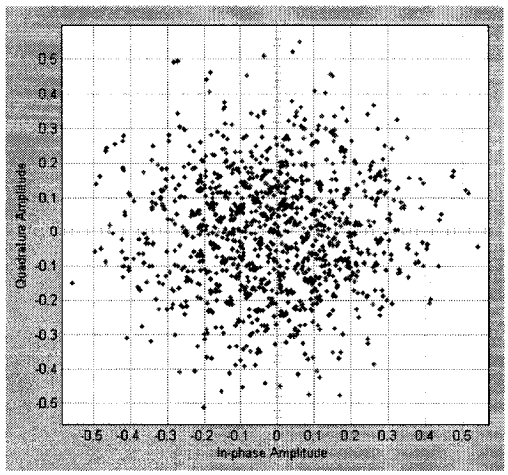
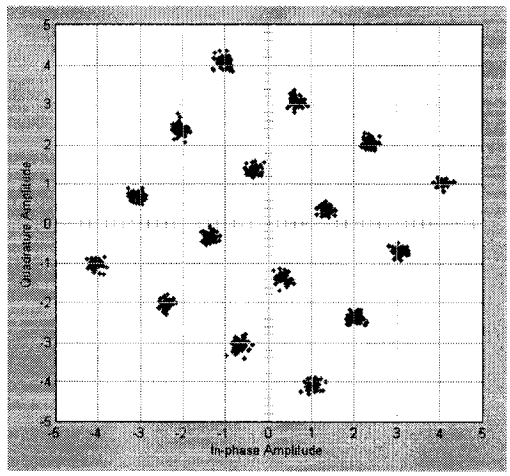


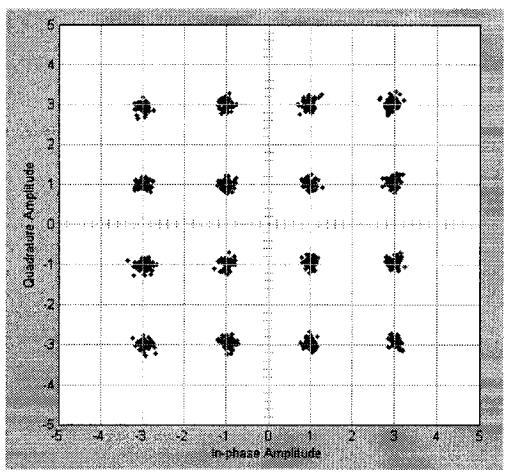
Figure 7.14 Simulation model for OFDM demodulation



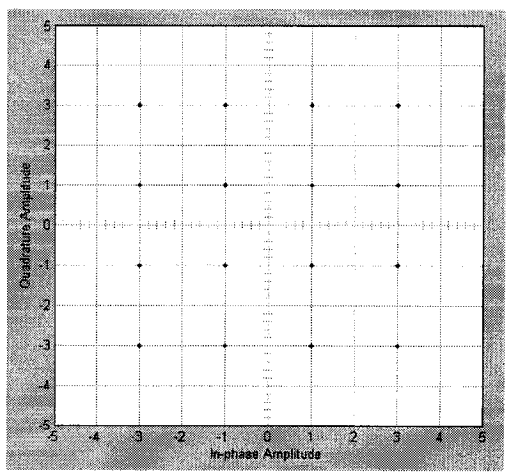
(a) six-port output signal



(b) decoded signal (distorted)



(c) recovered signal



(d) final output signal

Figure 7.15 Simulated output signal constellations for OFDM

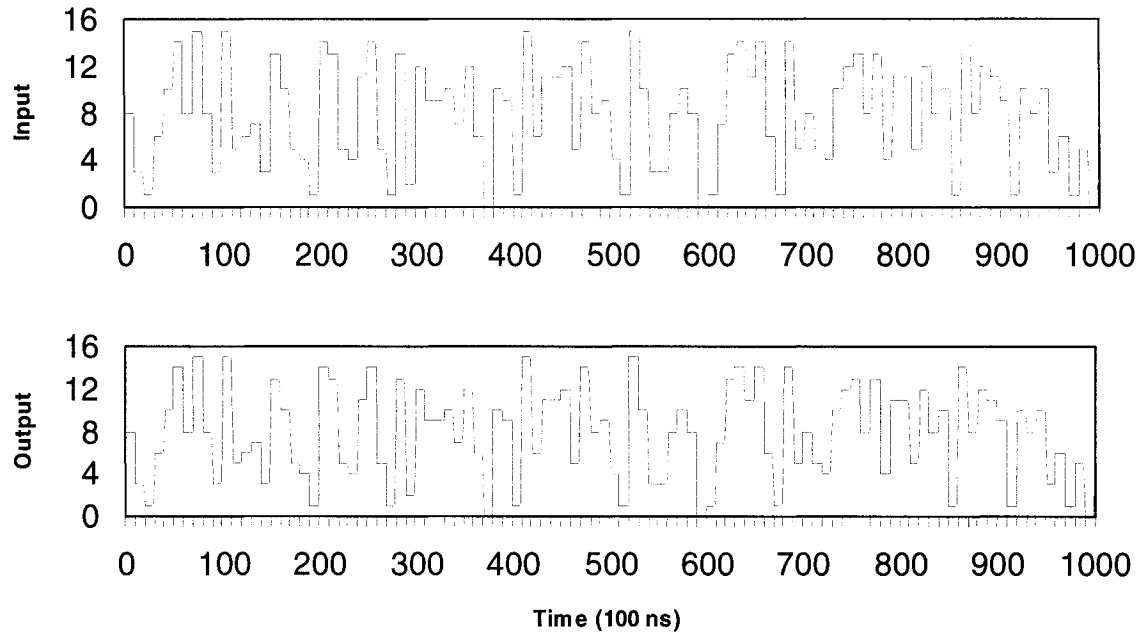
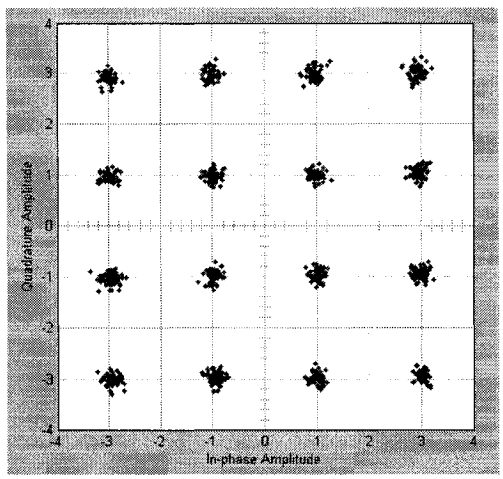
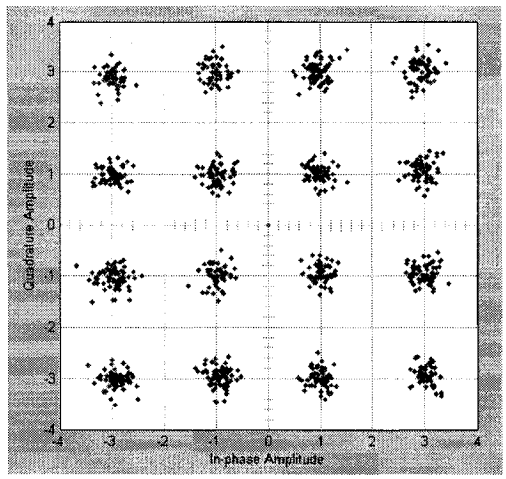


Figure 7.16 Simulated demodulation results of OFDM

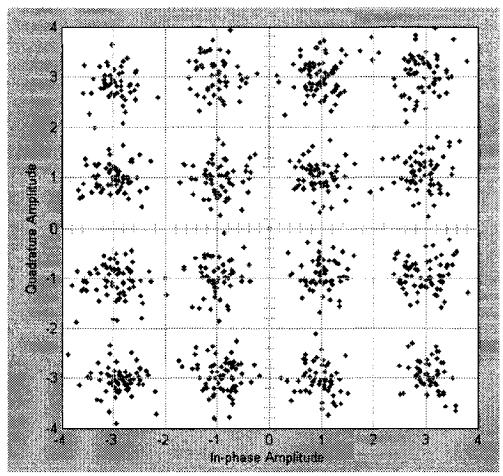
Figure 7.17 shows the simulated output OFDM signal constellations for various signal-to-noise ratios (SNR). The output signal constellations are presented in Figure 7.17 (a)–(c) for the OFDM signal with SNR equal to 10, 5, and 0 dB, respectively. Demodulation result after decision algorithm is presented in Figure 7.17(d).



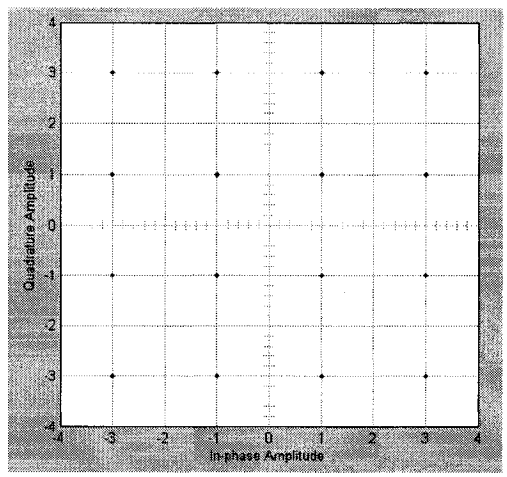
(a) SNR=10 dB



(b) SNR=5dB



(c) SNR=0dB



(d) demodulation result

Figure 7.17 Simulated output signal constellations for OFDM with different SNRs.

7.3 BER performance of six-port SDR receiver platform

7.3.1 Theoretical concepts

BER is one of the most important parameters to estimate the quality of a receiver system. Normally, the BER curve is given vs. E_b/N_0, where E_b is the average energy of a modulated bit and N_0 is the noise power spectral density. Before analyzing the BER performance of the proposed SDR receiver, some theoretical concepts are presented.

The probability of error P_e, is a function of the available carrier to noise (C/N) ratio in a stationary AWGN environment. The term "P_e" is most frequently used in theoretical references, whereas the practically equivalent term BER is used in applied references and specifications.

The given theoretical BER performance of QPSK modulation for an AWGN channel is summarized in equation (7.2)

$$P_e = \frac{1}{2} erfc \sqrt{\frac{E_b}{N_o}} \tag{7.2}$$

Where as mentioned before, E_b is the average energy of a modulated bit, N_0 is the noise power spectral density. The function *erfc* can be expressed as:

$$erfc(x) = \frac{2}{\sqrt{\pi}} \int_{x}^{\infty} \exp^{-\omega^2} \, d\omega \tag{7.3}$$

The ratio of required bit energy (E_b) to noise density (N_0) ratio (the E_b/N_0 ratio) is a convenient quantity for system calculations and performance comparisons. However, in practical measurements, it is more convenient to measure the average carrier-to-average noise power ratio. Most tests are performed using power meters and root-mean-square (rms) voltage meters, which are readily available. E_b/N_0 can be easily converted to C/N through the following relations:

Since

$$E_b = CT_b = C\left(\frac{1}{f_b}\right) \tag{7.4}$$

$$N_o = \frac{N}{B_W} \tag{7.5}$$

Here B_w is the receiver noise bandwidth, and f_b is system bit rate, so we have,

$$\frac{E_b}{N_o} = \frac{C/f_b}{N/B_W} = \frac{C}{N} \cdot \frac{B_W}{f_b} \tag{7.6}$$

Thus,

$$\left(\frac{E_b}{N_o}\right)_{dB} = \left(\frac{C}{N}\right)_{dB} + 10\log\frac{B_W}{f_b} \tag{7.7}$$

The E_b/N_0 ratio equals the product of the *C/N* ratio and the receiver noise bandwidth-to-bit rate ratio ($\frac{B_W}{f_b}$). Therefore, any C/N measuring instrument can be recalibrated to read E_b/N_0 directly.

For QPSK, the double-sideband RF noise bandwidth of the Nyquist-filtered system equals one half of the bit rate. There fore $f_b=2B_w$, so

$$\left(\frac{E_b}{N_o}\right)_{dB} = \left(\frac{C}{N}\right)_{dB} - 3dB \tag{7.8}$$

For QAM16, the theoretical BER performance for a stationary AWGN channel is given by.

$$P_e = \frac{3}{8} erfc\sqrt{\frac{2E_b}{9N_o}} \tag{7.9}$$

For QAM16, $f_b = 4B_w$. From (7.7), we have

$$\left(\frac{E_b}{N_o}\right)_{dB} = \left(\frac{C}{N}\right)_{dB} - 6dB \tag{7.10}$$

The theoretic BER curves vs. E_b/N_0 for QPSK and QAM16 are presented in Figure 7.18 and Figure 7.19.

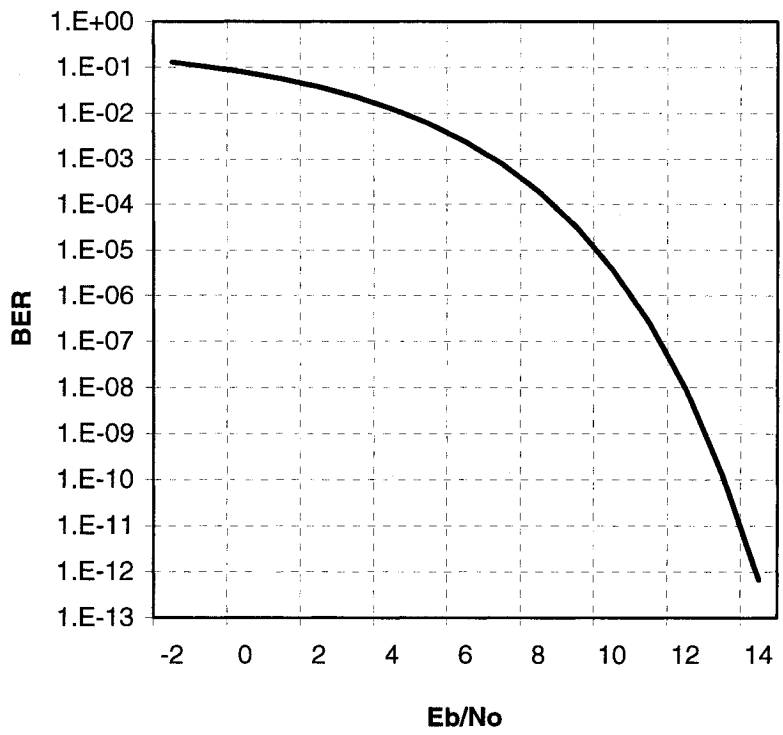


Figure 7.18 Theoretic BER for QPSK signal.

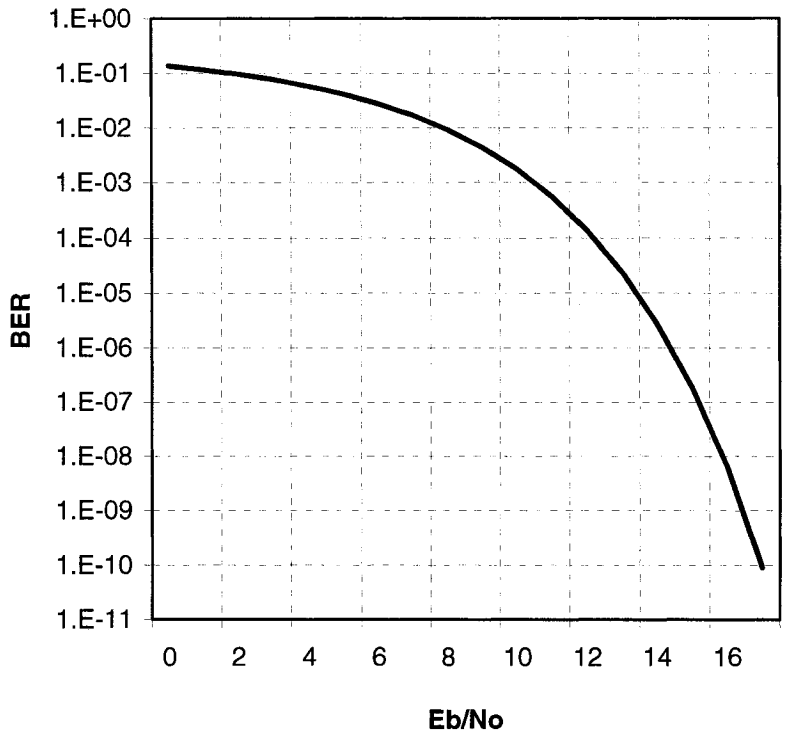


Figure 7.19 Theoretic BER for QAM16 signal.

7.3.2 BER measurement

The BER curves of the proposed six-port receiver are measured to test the system performance. Two modulation schemes (QPSK and QAM16) are selected for BER measurements. The block diagram of the BER measurement setup is described in Figure 7.20. A 1 Mbit/s pseudorandom bit sequence is generated from an Anritsu MP1630B BER analyzer and then fed to a vector signal modulator. QPSK/QAM16 modulated signals and reference signals of 250 MHz are generated using an HP-8782B vector signal modulator, then 24 GHz modulated RF signals and reference signals are obtained

from an Anrithsu MG3694A signal generator and two SU26A21D sideband up-converters. The power level of the RF modulated signal to the six-port is -20 dBm. The output signal from four power detectors are sent to two synchronized Altera FPGA DSP boards. The receiver algorithms are implemented in two FPGA processors. The BER analyzer receives the demodulated signal from DSP1 and evaluates the BER values of the receiver system. An additional white noise generator is applied for noise measurements.

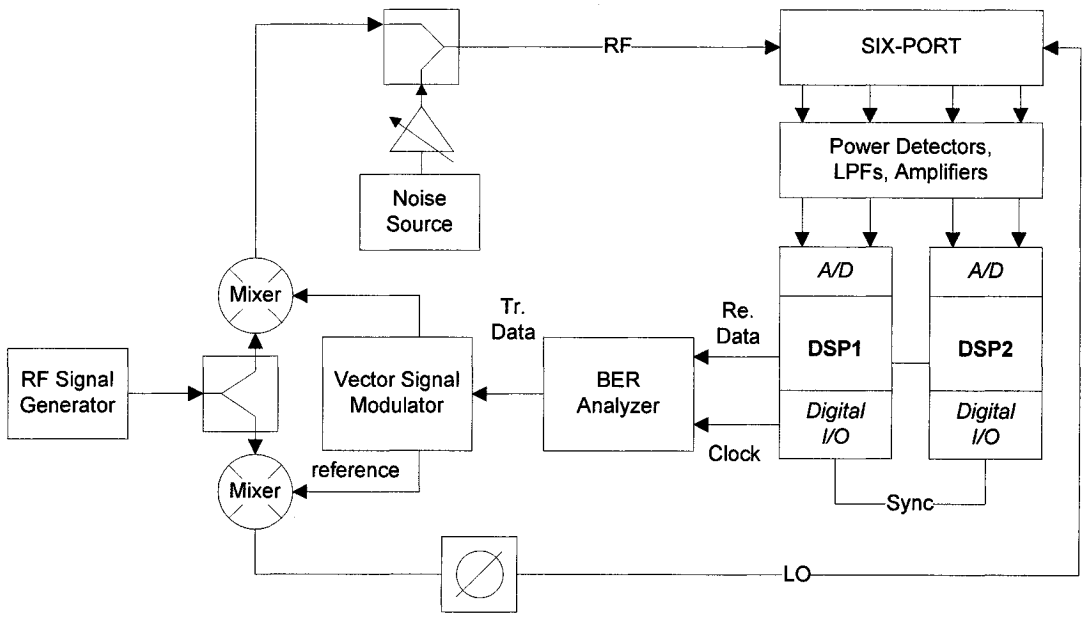


Figure 7.20 Block diagram of the BER measurement platform

Figure 7.21 is a photograph of a Stratix EP1S80 DSP development board with two A/Ds (12-bits sampling rate of 125 MHz) and D/As (14 bits sampling rate of 165 MHz),

FPGA chip (Altera EP1S80B956C6) and two digital input/output ports, configuration ports and external clock connector. Several DSP boards may be operated in parallel by the cabling digital I/O ports.

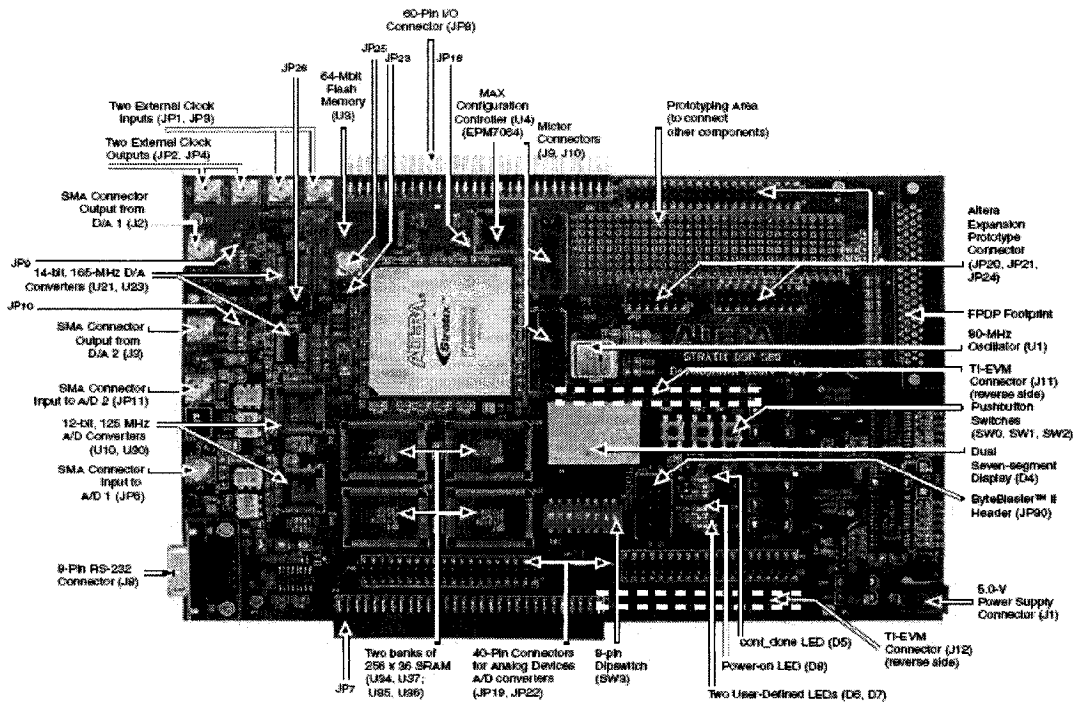


Figure 7.21 Photograph of Stratix EP1S80 DSP Development Board

Figure 7.22 shows a photograph of our test setup. It consists of an RF signal generator, a vector signal modulator, a DC power supply, an SIW six-port, an RF power divider and two RF up-converters, a baseband amplifier board and two FPGA development boards.

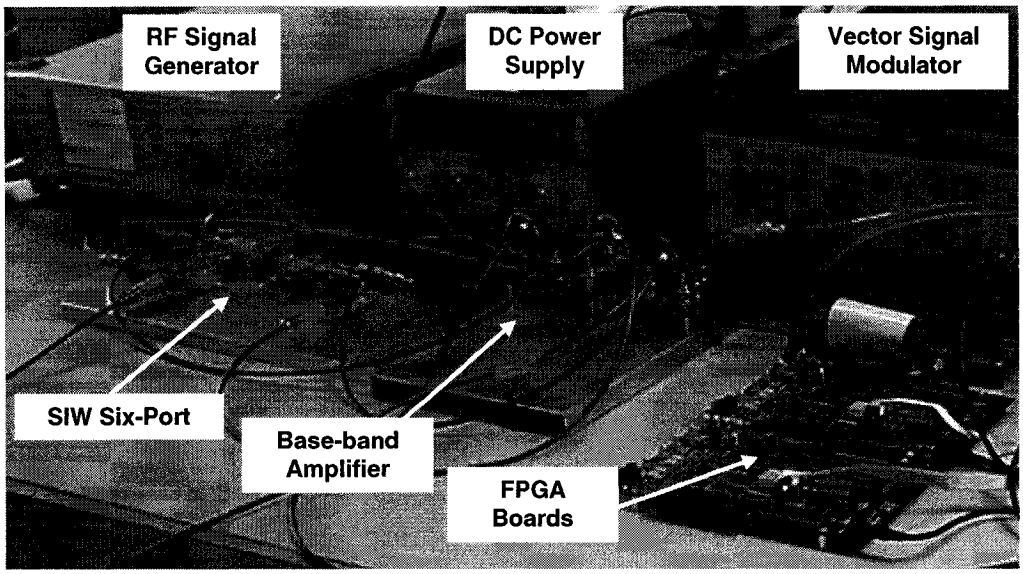


Figure 7.22 Test bed setup for receiver performance evaluation

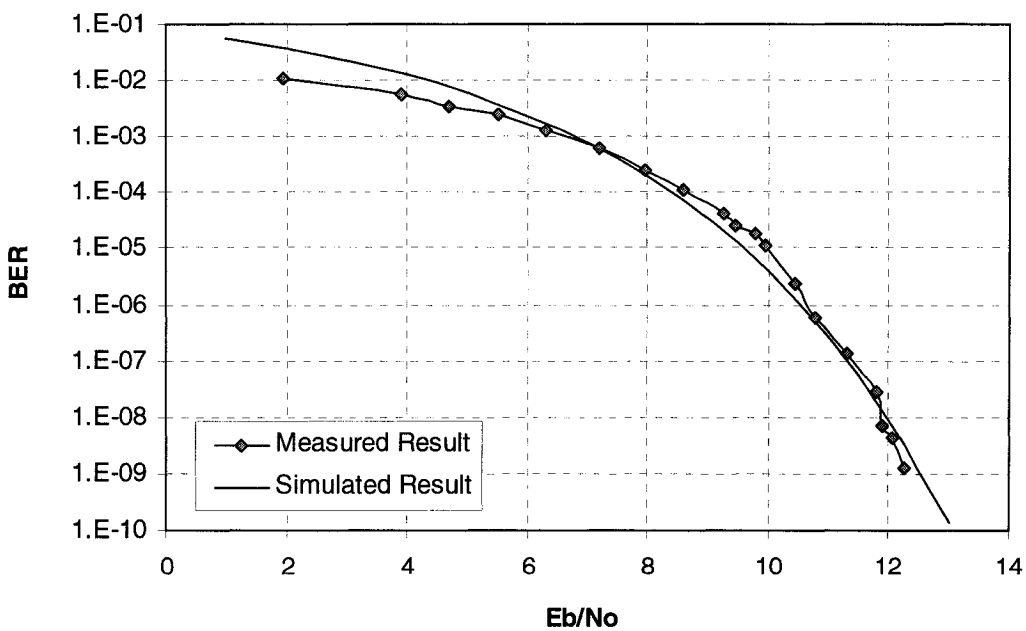


Figure 7.23 Simulated and measured BER for QPSK signal.

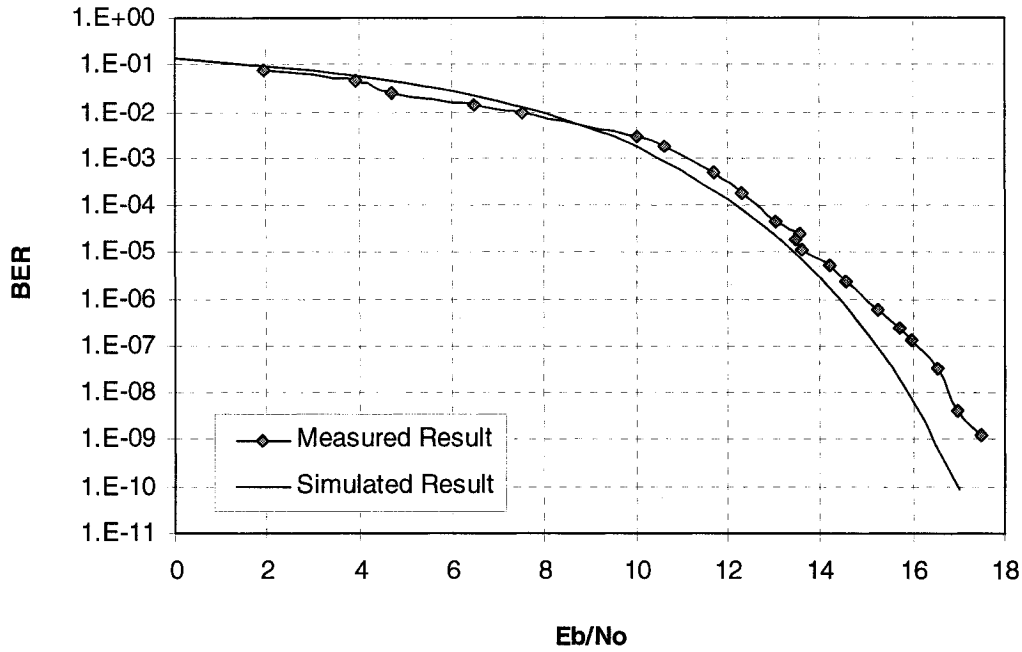


Figure 7.24 Simulated and measured BER for QAM16 signal.

Simulated and measured BER vs. E_b/N_0 for the two modulation types are presented in Figure 7.23 and Figure 7.24. The signal bit rate is 1 Mb/s. It can be seen that the simulated BER curve and measured BER curve are in excellent agreement, the BER is less than 1E-6 when E_b/N_0 is higher than 10.5 dB (QPSK) and 15 dB (QAM16).

CHAPTER VIII

CONCLUSION

A universal SDR receiver platform based on six-port technology has been proposed and presented. This receiver can support multi-modulation and multi-band communication and intends to achieve comparable performance as existing super-heterodyne receiver. This platform scheme is strongly motivated by the fact that the speed and performance of the state of the art re-configurable devices, such as DSP and FPGA, are very promising and the price will be significantly reduced, while the cost of the microwave components are relatively stable. The receiver configuration shifts the complexity to the digital signal processing part and alleviates problems associated with RF components; therefore, it will be better-off in terms of cost and functionality in the long run.

The proposed six-port SDR receiver scheme falls into the direct conversion receiver category. Historically, this type of receiver played insignificant role due to some of its inherent drawbacks. The six-port SDR receiver makes it possible to improve the direct receiver performance which can be stated as follows:

- In early days, amplification of an RF signal was so expensive that it had to be carried out at a low frequency, i.e. IF. As the technology advanced, low-cost high-gain microwave transistors have become available such that the cost of these

transistors is no longer a major factor in the overall design of a receiver. This makes it easier than ever to adopt a direct receiver configuration.

- Wide band microwave amplifier design techniques have matured to maintain uniform gain and noise figure over a wide frequency band. The sensitivity non-uniformity of the early direct receiver has been overcome.

- Six-port calibration eliminates most of the errors related to imperfect circuit fabrication to allow the six-port receiver operating at RF frequency without any compromise with regards to accuracy. Besides, coding technology can be introduced to reduce the BER of the receiver.

- The recent development of VLSI and ASIC technology makes the high speed digital signal processing practical and cost-effective. This is the main impetus behind the emergence of the SDR receiver.

The research work described in this dissertation has bridged a gap between six-port technology and emerging SDR field. It is proven through a number of computer simulations and measurements that the combination of SDR and six-port technology provides a great flexibility in system configuration, a significant reduction in system development cost, and also a high potential for software reuse. A MHMIC microstrip six-port circuit and an SIW six-port circuit are designed and fabricated. The transmission characteristics are simulated and measured. The results of BER vs. E_b/N_0 of the SDR

receiver for different modulation schemes have been described. The simulated and measured results proved that the proposed receiver is flexible and stable, showing a possible direct demodulator for future SDR terminals in various wireless communication systems.

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